ArmSoM-AIM7

ArmSoM-AIM7_V1.0

Main Functions Introduction

1) PMIC: 1xRK806-1
2) RAM: 2xLPDDR4/4X_32bit
3) ROM: eMMC5.1
4) Support: 1 x TYPEC3.0+ 2 x USB2.0 HOST+ 1 x USB2.0 OTG
5) Support: 1 x 4Lane PCIe3.0 Connector + 1 x 1Lane PCIe2.0 Connector
6) Support: 1 x 4Lanes DP Port
7) Support: 1 x HDMI2.1 TX or 1 x eDP1.4 TX
8) Support: 4 x 2Lanes MIPI DPHY RX Camera
9) Support: 1 x 4Lanes MIPI D/CPHY RX Camera
10) Support: 1 x 2Lanes MIPI D/CHY-TX
11) Support: 1 x SDMMC3.0 Card
12) Support: 1 x 10/100/1000 RJ45 Port(RGMII)
13) Support: 15 x GPIO
14) Support: 2 x I2S
15) Support: 4 x I2C
16) Support: 2 x SPI
17) Support: 3 x UART

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	01.Cover Page				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	1 of 24

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Description

Note

Option

Generate Bill of Materials

Header:

Item\tPart\tDescription\tPCB Footprint\tReference\tQuantity\tOption

Combined property string:

{Item}\t{Value}\t{Description}\t{PCB Footprint}\t{Reference}\t{Quantity}\t{Option}

Notes

NOTE 1:
Component parameter description
1. DNP stands for component not mounted temporarily
2. If Value or option is DNP, which means the area is reserved without being mounted

NOTE 2:
Please use our recommended components to avoid too many changes.
For more informations about the second source,please refer to our AVL.

Note

The power suffix S0 or S3 means:

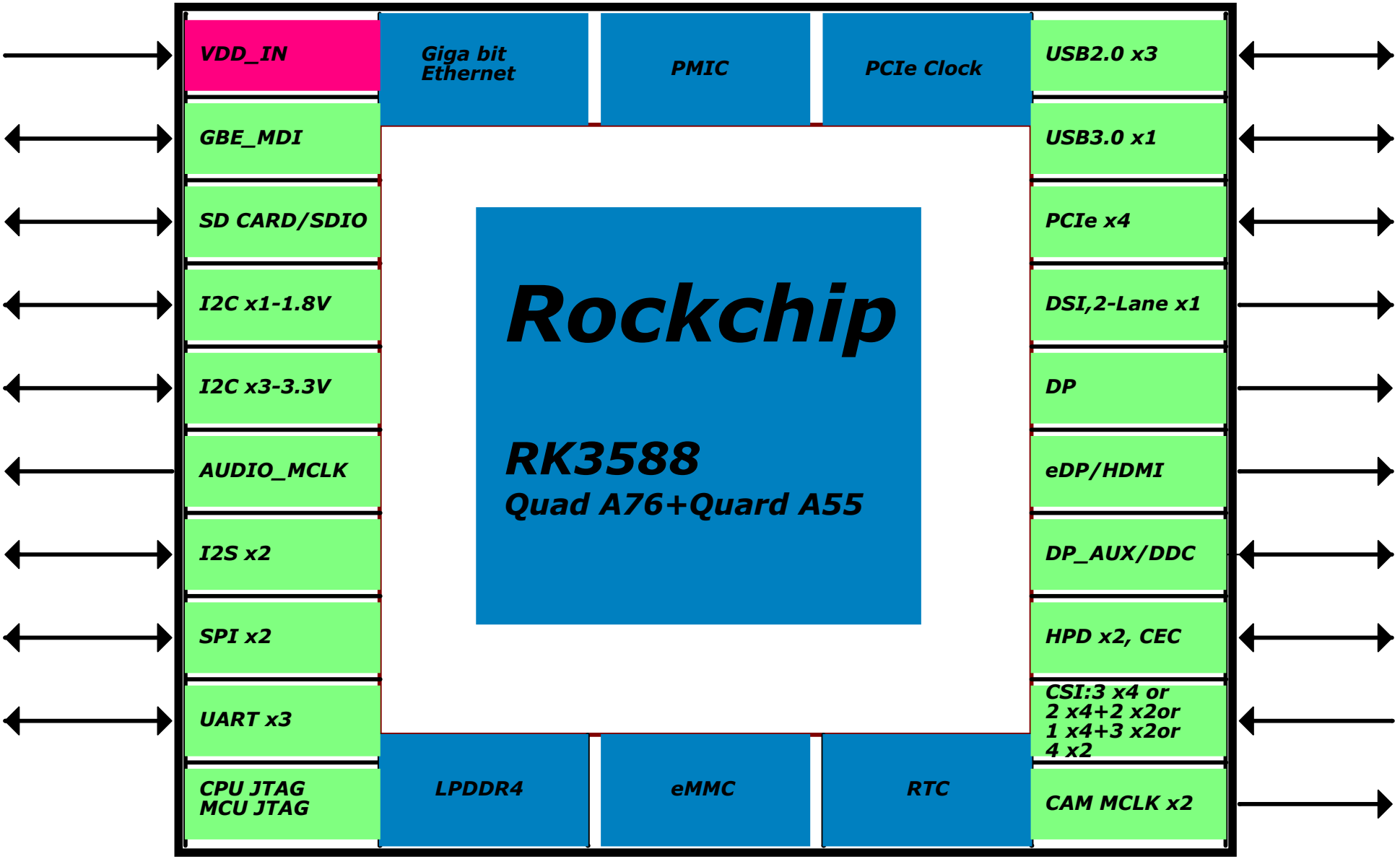
S3: Keep power On during sleeping

S0:Power off during sleeping

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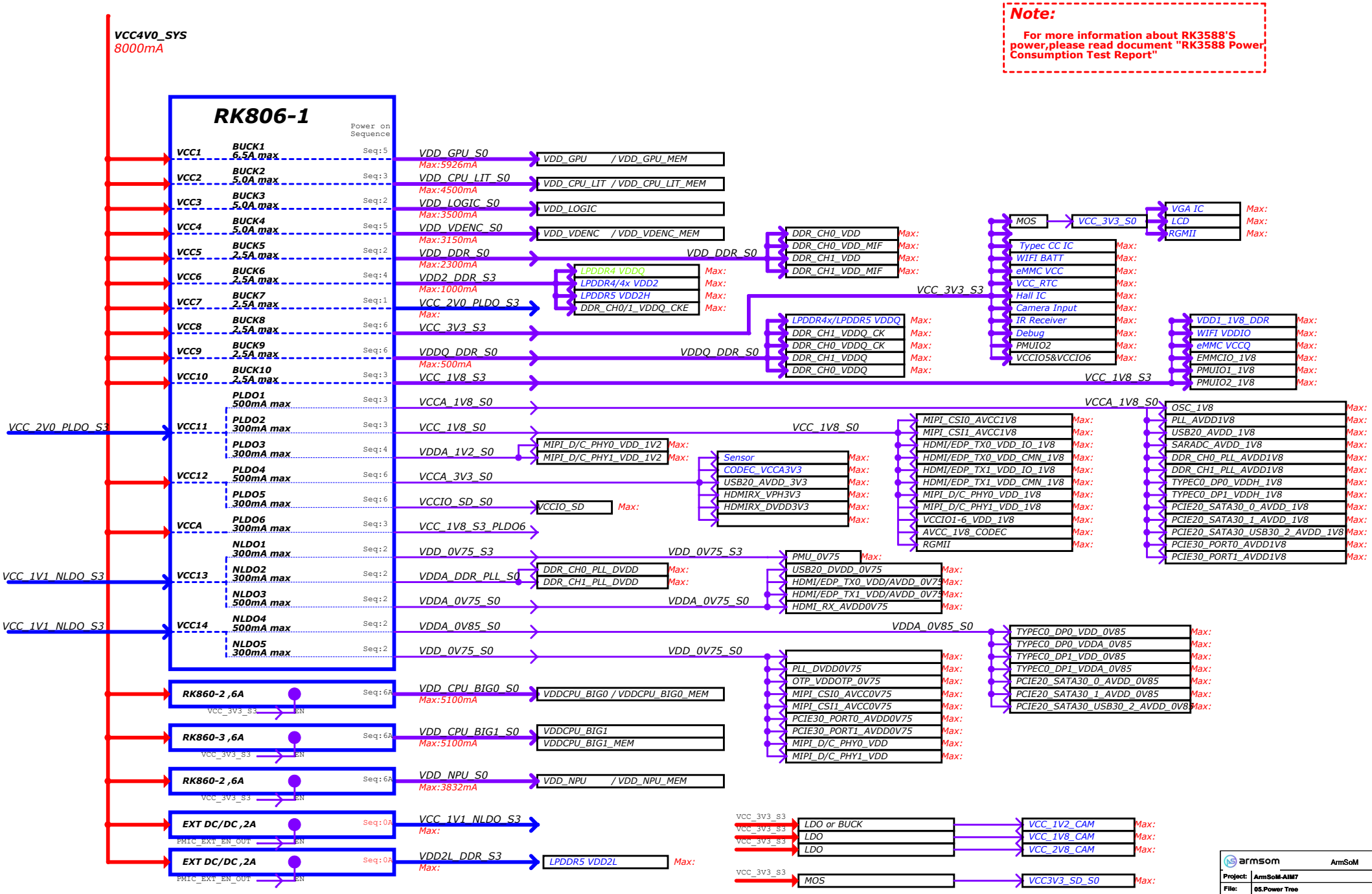
Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2023-11-03	Liu Xinglin	alpha version	

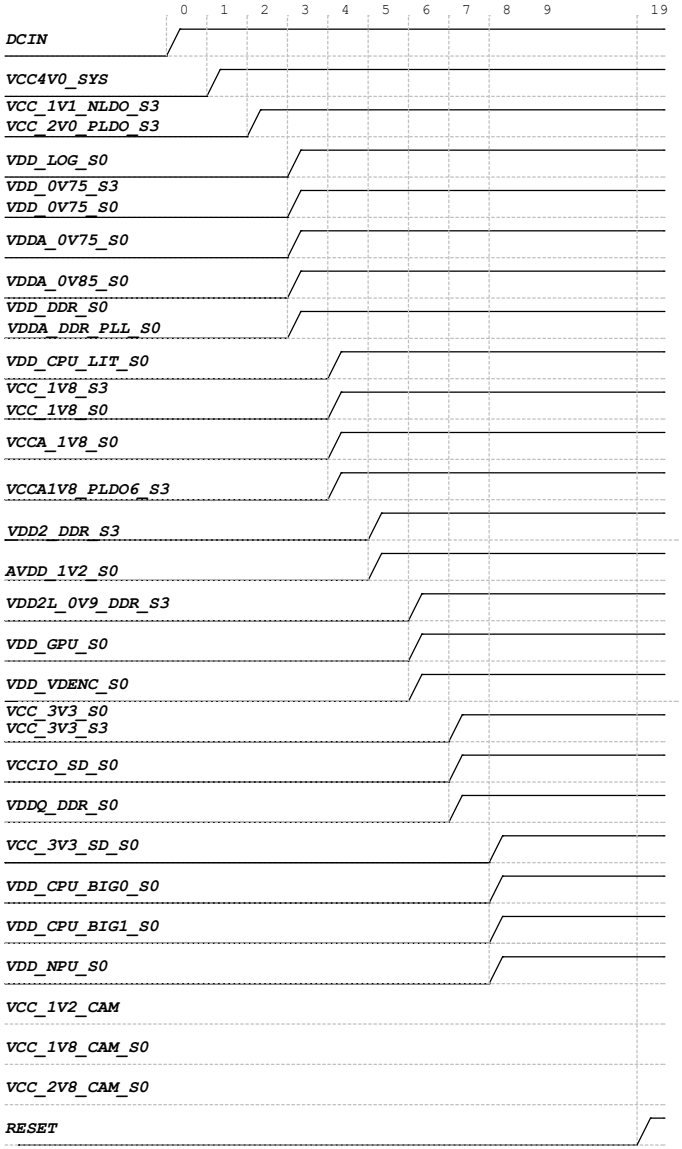


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File:	04.Block Diagram				
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Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	4 of 24

Power Tree


Note:
For more information about RK3588'S power,please read document "RK3588 Power Consumption Test Report"
VCC4V0_SYS
8000mA
RK806-1
Power on Sequence
VCC1 BUCK1 6.5A max Seq:5 VDD_GPU_S0 Max:5926mA
VCC2 BUCK2 5.0A max Seq:3 VDD_CPU_LIT_S0 Max:4500mA
VCC3 BUCK3 5.0A max Seq:2 VDD_LOGIC_S0 Max:3500mA
VCC4 BUCK4 5.0A max Seq:5 VDD_VDENC_S0 Max:3150mA
VCC5 BUCK5 2.5A max Seq:2 VDD_DDR_S0 Max:2300mA
VCC6 BUCK6 2.5A max Seq:4 VDD2_DDR_S3 Max:1000mA
VCC7 BUCK7 2.5A max Seq:1 VCC_2V0_PLDO_S3 Max:
VCC8 BUCK8 2.5A max Seq:6 VCC_3V3_S3
VCC9 BUCK9 2.5A max Seq:6 VDDQ_DDR_S0 Max:500mA
VCC10 BUCK10 2.5A max Seq:3 VCC_1V8_S3
VCC11 PLDO1 500mA max Seq:3 VCCA_1V8_S0
PLDO2 300mA max Seq:3 VCC_1V8_S0
PLDO3 300mA max Seq:4 VDDA_1V2_S0
VCC12 PLDO4 500mA max Seq:6 VCCA_3V3_S0
PLDO5 300mA max Seq:6 VCCIO_SD_S0
VCCA PLDO6 300mA max Seq:3 VCC_1V8_S3_PLDO6
NLDO1 300mA max Seq:2 VDD_0V75_S3
VCC13 NLDO2 300mA max Seq:2 VDDA_DDR_PLL_S0
NLDO3 500mA max Seq:2 VDDA_0V75_S0
VCC14 NLDO4 500mA max Seq:2 VDDA_0V85_S0
NLDO5 300mA max Seq:2 VDD_0V75_S0
RK860-2 ,6A Seq:6A VDD_CPU_BIG0_S0 Max:5100mA
RK860-3 ,6A Seq:6A VDD_CPU_BIG1_S0 Max:5100mA
RK860-2 ,6A Seq:6A VDD_NPU_S0 Max:3832mA
EXT DC/DC ,2A Seq:0A VCC_1V1_NLDO_S3 Max:
EXT DC/DC ,2A Seq:0A VDD2L_DDR_S3 Max:
VCC_3V3_S3
EN
PMIC_EXT_EN_OUT
VCC_2V0_PLDO_S3
VCC_1V1_NLDO_S3
VCC_1V1_NLDO_S3
VDD_GPU / VDD_GPU_MEM
VDD_CPU_LIT / VDD_CPU_LIT_MEM
VDD_LOGIC
VDD_VDENC / VDD_VDENC_MEM
VDD_DDR_S0
LPDDR4 VDDQ
LPDDR4/4x VDD2
LPDDR5 VDD2H
DDR_CH0/1_VDDQ_CKE
VCC_3V3_S3
LPDDR4x/LPDDR5 VDDQ
DDR_CH1_VDDQ_CK
DDR_CH0_VDDQ_CK
DDR_CH1_VDDQ
DDR_CH0_VDDQ
VDDQ_DDR_S0
DDR_CH0_VDD
DDR_CH0_VDD_MIF
DDR_CH1_VDD
DDR_CH1_VDD_MIF
MOS
VCC_3V3_S0
VGA IC
LCD
RGMII
Typec CC IC
WIFI BATT
eMMC VCC
VCC_RTC
Hall IC
Camera Input
IR Receiver
Debug
PMUIO2
VCCIO5&VCCIO6
VCC_1V8_S3
VDD1_1V8_DDR
WIFI VDDIO
eMMC VCCQ
EMMCIO_1V8
PMUIO1_1V8
PMUIO2_1V8
VCCA_1V8_S0
OSC_1V8
PLL_AVDD1V8
USB20_AVDD_1V8
SARADC_AVDD_1V8
DDR_CH0_PLL_AVDD1V8
DDR_CH1_PLL_AVDD1V8
TYPEC0_DP0_VDDH_1V8
TYPEC0_DP1_VDDH_1V8
PCIE20_SATA30_0_AVDD_1V8
PCIE20_SATA30_1_AVDD_1V8
PCIE20_SATA30_USB30_2_AVDD_1V8
PCIE30_PORT0_AVDD1V8
PCIE30_PORT1_AVDD1V8
MIPI_D/C_PHY0_VDD_1V2
MIPI_D/C_PHY1_VDD_1V2
Sensor
CODEC_VCCA3V3
USB20_AVDD_3V3
HDMIRX_VPH3V3
HDMIRX_DVDD3V3
VCCIO_SD
VCC_1V8_S0
MIPI_CSI0_AVCC1V8
MIPI_CSI1_AVCC1V8
HDMI/EDP_TX0_VDD_IO_1V8
HDMI/EDP_TX0_VDD_CMN_1V8
HDMI/EDP_TX1_VDD_IO_1V8
HDMI/EDP_TX1_VDD_CMN_1V8
MIPI_D/C_PHY0_VDD_1V8
MIPI_D/C_PHY1_VDD_1V8
VCCIO1-6_VDD_1V8
AVCC_1V8_CODEC
RGMII
DDR_CH0_PLL_DVDD
DDR_CH1_PLL_DVDD
VDD_0V75_S3
PMU_0V75
USB20_DVDD_0V75
HDMI/EDP_TX0_VDD/AVDD_0V75
HDMI/EDP_TX1_VDD/AVDD_0V75
HDMI_RX_AVDD0V75
VDDA_0V75_S0
VDDA_0V85_S0
TYPEC0_DP0_VDD_0V85
TYPEC0_DP0_VDDA_0V85
TYPEC0_DP1_VDD_0V85
TYPEC0_DP1_VDDA_0V85
PCIE20_SATA30_0_AVDD_0V85
PCIE20_SATA30_1_AVDD_0V85
PCIE20_SATA30_USB30_2_AVDD_0V85
PLL_DVDD0V75
OTP_VDDOTP_0V75
MIPI_CSI0_AVCC0V75
MIPI_CSI1_AVCC0V75
PCIE30_PORT0_AVDD0V75
PCIE30_PORT1_AVDD0V75
MIPI_D/C_PHY0_VDD
MIPI_D/C_PHY1_VDD
VDDCPU_BIG0 / VDDCPU_BIG0_MEM
VDDCPU_BIG1
VDDCPU_BIG1_MEM
VDD_NPU / VDD_NPU_MEM
LPDDR5 VDD2L
LDO or BUCK
LDO
LDO
MOS
VCC_1V2_CAM
VCC_1V8_CAM
VCC_2V8_CAM
VCC3V3_SD_S0
Max:
armsom
ArmSoM
Project: ArmSoM-AIM7
File: 05.Power Tree
Date: Wednesday, December 20, 2023
Rev: V1.0
Designed by: Liu Xinglin
Reviewed by: <Checker>
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Power Sequence



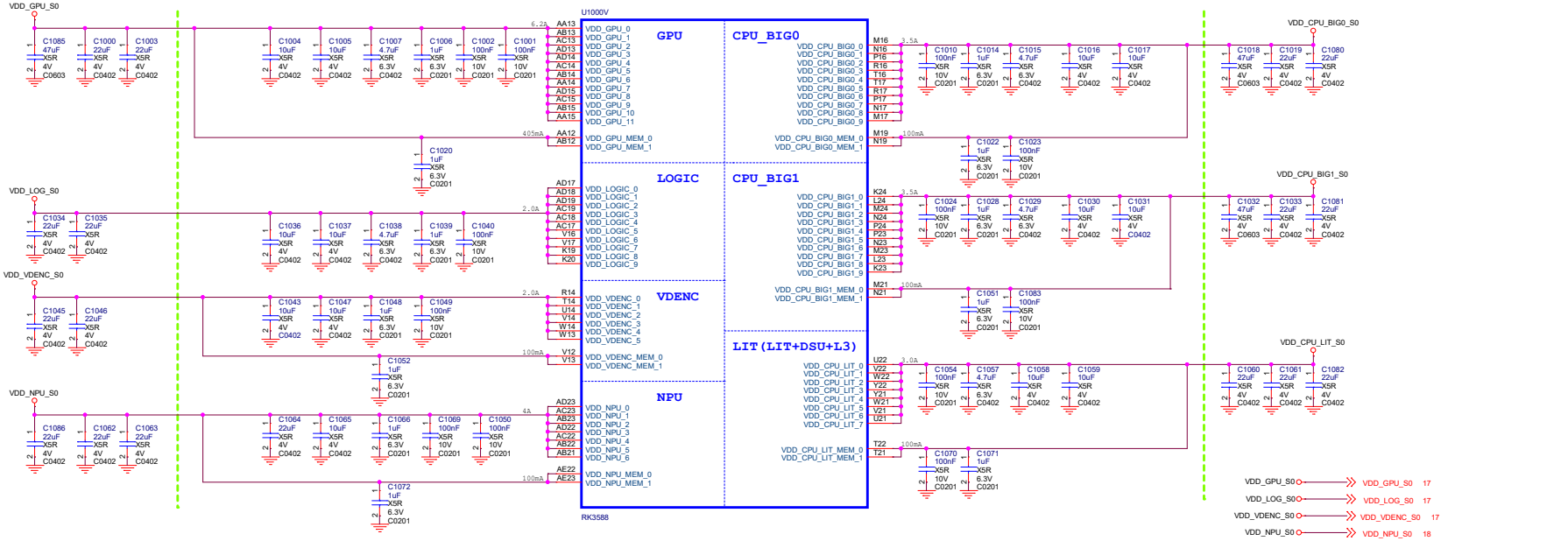
Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC4V0_SYS	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO	RK806-1_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC4V0_SYS	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC4V0_SYS	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_3V3_S3	EXT_BUCK	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_3V3_S3	LDO_PT5108	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

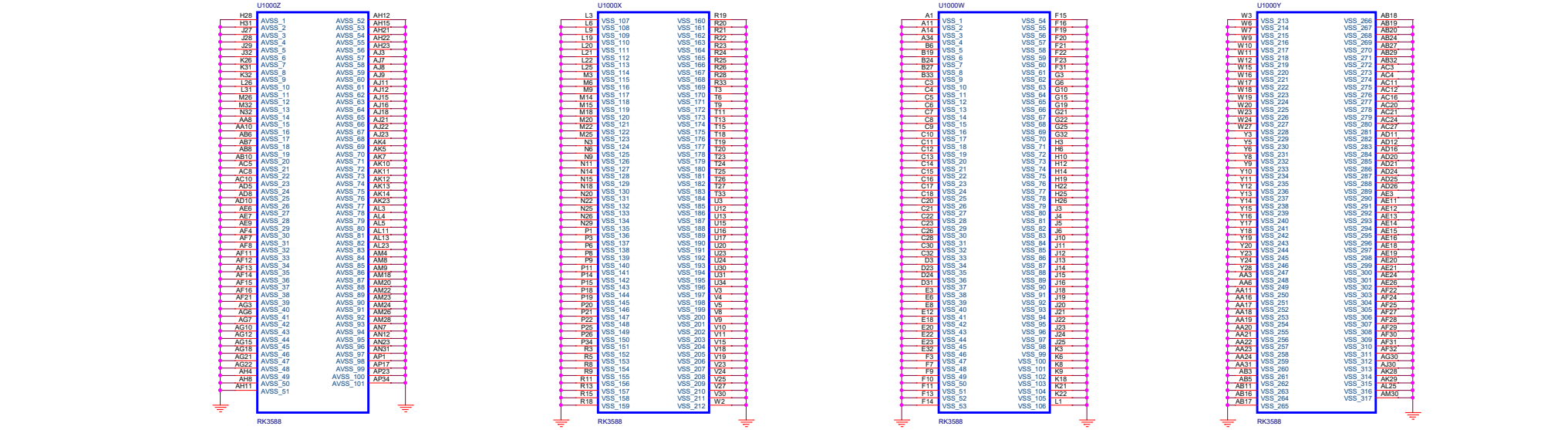
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	IO Operating Voltage
PMUIO1	Pin N28	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin R27 Pin P28	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3	1.8V
EMMCIO	Pin V26	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin G20	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AA7 Pin Y7	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V/3.3V
VCCIO3	Pin Y26	1.8V Only	VCCIO3_1V8	VCC_1V8_S0	1.8V
VCCIO4	Pin H20 Pin H21	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_1V8_S0	1.8V
VCCIO5	Pin W25 Pin W26	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_3V3_S0	3.3V
VCCIO6	Pin AC25 Pin AC26	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	3.3V

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Project:	ArmSoM-AIM7				
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RK3588_V(POWER)





armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	07.RK3588_Power/GND		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
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RK3588_E(OSC/PLL/PMUIO1/2)

Note:
Adjusted the load capacitance according to the crystal specification

The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF

Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

U1000E

OSC
XOUT_24M
XIN_24M

R1101 22R R0201 5%
Y1100 24MHz SMD3225-4P
C1101 18pF C0G 25V C0201
R1103 510K 5% R0201
C1102 18pF C0G 25V C0201
XOUT24M T34
XIN24M R34

PLL
OSC_1V8 N27
PLL_DVDD0V75 V20
PLL_AVDD1V8 U18
PLL_AVSS U19

VCCA_1V8_S0
VDD_0V75_S0
C1103 1uF C0201 X5R 4V
C1104 100nF C0201 X5R 6.3V
C1105 1uF C0201 X5R 4V
C1106 100nF C0201 X5R 6.3V
C1109 100nF C0201 X5R 6.3V

9,11,12,15,17 VCCA_1V8_S0 — VCCA_1V8_S0
12,13,15,17 VDD_0V75_S0 — VDD_0V75_S0
10,17,19,20,21,24 VCC_1V8_S3 — VCC_1V8_S3
17 VDD_0V75_S3 — VDD_0V75_S3
17,18,19,21,24 VCC_3V3_S3 — VCC_3V3_S3
1,11,12,13,14,15,16,17,18,19,20,21,22,23,24 GND

RK3588

PMUIO1 Domain
Operating Voltage=1.8V Only

NPOR_u M31 RESET_L — R1100 0R R0201 5% — TSADC_SHUT_H — RESET_L 17,24
C1100 100nF C0201 X5R 6.3V
TVSS M29

	REFCLK_OUT	/ GPIO0_A0_d	P33		MOD_SLEEP 24
TSADC_SHUT_ORG	/ TSADC_SHUT	/ GPIO0_A1_z	P32	TSADC_SHUT_H	
	PMIC_SLEEP1	/ GPIO0_A2_d	R32		PMIC_PWR_CTRL1 17
	PMIC_SLEEP2	/ GPIO0_A3_d	R31		CPU_BIG0_VSEL 18
	SDMMC_DET	/ GPIO0_A4_u	P31		SDMMC_DET_L 24
PMU_DEBUG	/ SDMMC_PWREN	/ SPI2_CLK_M2	/ GPIO0_A5_d	N31	R1104 22R 5% R0201 — PMIC_SPI_CLK 17
	I2C0_SDA_M0	/ SPI2_MOSI_M2	/ GPIO0_A6_z	N30	R1107 22R 5% R0201 — PMIC_SPI_MOSI 17
	PMIC_INT_L		/ GPIO0_A7_u	M30	PMIC_INT_L 17
UART0_RX_M1	/ I2C1_SCL_M1	/ SPI2_CS1_M2	/ GPIO0_B0_z	L30	RTC_INT_L 19
PWM5_M0 / UART0_TX_M1	I2C1_SDA_M1	/ SPI2_CS0_M2	/ GPIO0_B1_z	K30	PMIC_SPI_CS 17
	CLK32K_OUT0	/ CLK32K_IN	/ GPIO0_B2_u	K29	GPIO0_B2 24
	I2C0_SCL_M0	/ SPI2_MISO_M2	/ GPIO0_B3_z	L29	

PMUIO1_1V8 N28 — C1107 100nF C0201 X5R 6.3V — VCC_1V8_S3

PMUIO1/2 Domain Logic Power
Operating Voltage=0.75V

PMU_0V75 P27 — C1110 100nF C0201 X5R 6.3V — C1111 1uF C0201 X5R 4V — VDD_0V75_S3

RK3588_F(PMUIO2)

U1000F

PMUIO2 Domain
Operating Voltage=1.8V/3.3V

	UART2_TX_M0			I2S1_MCLK_M1	PCIE30X1_1_CLKREQN_M0		I2C1_SCL_M0	JTAG_TCK_M2	/GPIO0_B5_d
	UART2_RX_M0			I2S1_SCLK_M1	PCIE30X1_1_WAKEN_M0		I2C1_SDA_M0	JTAG_TMS_M2	/GPIO0_B6_d
		CAN0_TX_M0		I2S1_LRCK_M1	PCIE30X1_1_PERSTN_M0	SPI0_CS1_M0	I2C2_SCL_M0	PWM0_M0	/GPIO0_B7_d
		CAN0_RX_M0	PDM0_CLK0_M1		PCIE30X1_0_CLKREQN_M0	SPI0_MOSI_M0	I2C2_SDA_M0	PWM1_M0	/GPIO0_C0_d
								PMIC_SLEEP3	/GPIO0_C1_d
								PMIC_SLEEP4	/GPIO0_C2_d
								PMIC_SLEEP5	/GPIO0_C3_d
	UART0_RX_M0	DP0_HPDIN_M1	PDM0_CLK1_M1		PCIE30X1_0_WAKEN_M0		I2C4_SDA_M2	PWM2_M0	/GPIO0_C4_d
PWM4_M0	UART0_TX_M0	DP1_HPDIN_M1		I2S1_SDI0_M1	PCIE30X1_0_PERSTN_M0		I2C4_SCL_M2	GPU_AVS	/GPIO0_C5_u
PWM5_M1	UART0_RTSN	SATA_CP_POD		I2S1_SDI1_M1	PCIE30X4_CLKREQN_M0	SPI0_CLK_M0		NPU_AVS	/GPIO0_C6_u
	UART1_RTSN_M2		PDM0_SDI0_M1	I2S1_SDI2_M1	PCIE30X4_WAKEN_M0	SPI0_MISO_M0	I2C6_SDA_M0	PWM6_M0	/GPIO0_C7_d
	UART1_CTSN_M2		PDM0_SDI1_M1	I2S1_SDI3_M1	PCIE30X4_PERSTN_M0	SPI3_MISO_M2	I2C6_SCL_M0	PWM7_IR_M0	/GPIO0_D0_d
HDMI_TX0_CEC_M1	UART1_TX_M2	UART0_CTSN	HDMI_RX_SDA_M0	I2S1_SDO0_M1	PCIE30X2_CLKREQN_M0	SPI0_CS0_M0	I2C0_SCL_M2	CPU_BIG0_AVS	/GPIO0_D1_u
HDMI_TX1_CEC_M1	UART1_RX_M2		HDMI_RX_SCL_M0	I2S1_SDO1_M1	PCIE30X2_WAKEN_M0	SPI3_MOSI_M2	I2C0_SDA_M2		/GPIO0_D2_u
						SPI3_CLK_M2		LITCPU_AVS	/GPIO0_D3_u
HDMI_TX0_SDA_M1	SATA_CPDET	CAN2_RX_M1	PDM0_SDI2_M1	I2S1_SDO2_M1	PCIE30X2_PERSTN_M0	SPI3_CS0_M2	I2C1_SCL_M2	PWM3_IR_M0	/GPIO0_D4_u
HDMI_TX0_SCL_M1	SATA_MP_SWITCH	CAN2_TX_M1		I2S1_SDO3_M1		SPI3_CS1_M2	I2C1_SDA_M2	CPU_BIG1_AVS	/GPIO0_D5_u
			PDM0_SDI3_M1					PMIC_SLEEP6	/GPIO0_D6_d

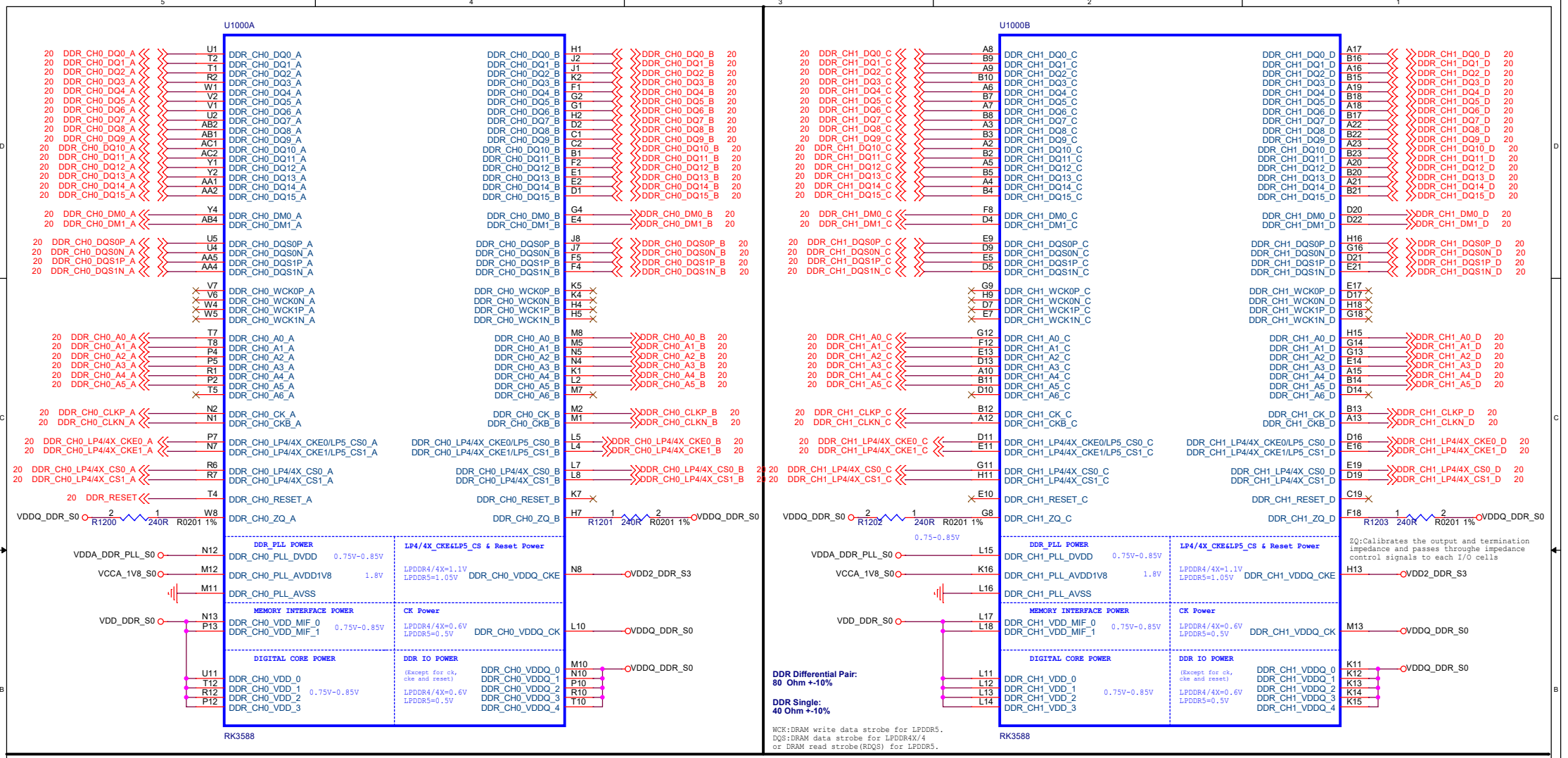
P29 UART2_TX_M0 24
R29 UART2_RX_M0 24
T28 I2C2_SCL_M0 24
T31 I2C2_SDA_M0 24
U32 NPU_VSEL 18
T32 GPU PMIC_PWR_CTRL3 17
T30 DDR R1115 1 100K 2 R0201 — PMIC_PWR_CTRL2 17
R1116 120K R0201
R30 I2C4_SDA_M2 24
P30 I2C4_SCL_M2 24
T29 PCIE30X4_CLKREQn_M0 23,24
V31 PCIE30X4_WAKEn_M0 24
W31 PCIE30X4_PERSTn_M0 24
W30 I2C0_SCL_M2 18
W29 I2C0_SDA_M2 18
U33 GPIO0_D3 24
V29 I2C1_SCL_M2 18
V28 I2C1_SDA_M2 18
W28 CPU_BIG1_VSEL 18

VCC_3V3_S3
R1113 2.2K 5% R0201 — R1114 2.2K 5% R0201 — I2C1_SCL_M2 — I2C1_SDA_M2
VCC_3V3_S3
R1139 2.2K 5% R0201 — R1140 2.2K 5% R0201 — I2C0_SCL_M2 — I2C0_SDA_M2
VCC_3V3_S3
R1910 2.2K R0201 — R1911 2.2K R0201 — I2C4_SDA_M2 — I2C4_SCL_M2
VCC_3V3_S3
R1912 2.2K R0201 — R1913 2.2K R0201 — I2C2_SCL_M0 — I2C2_SDA_M0

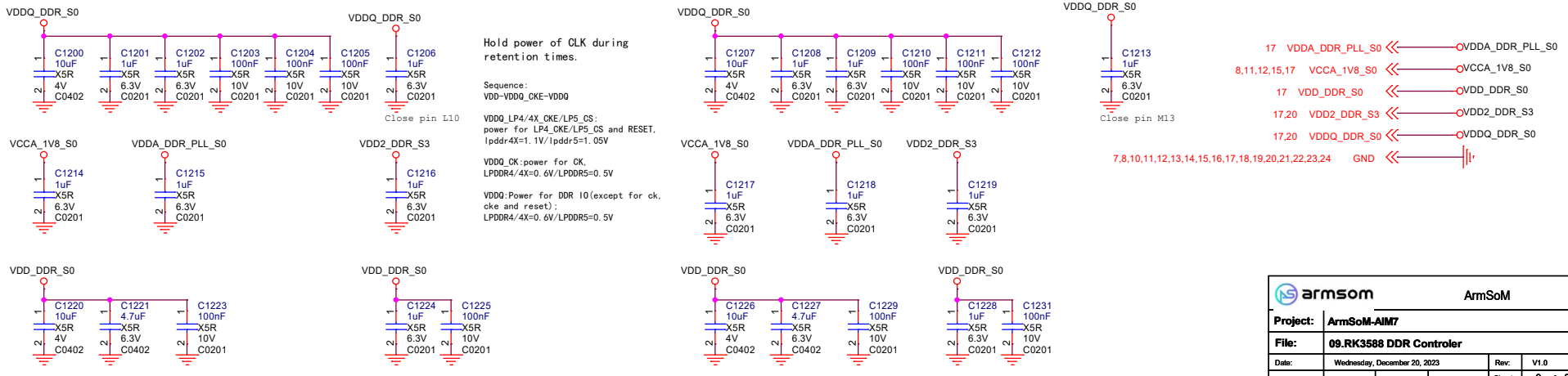
PMUIO2_1V8 R27 — C1112 100nF X5R 6.3V C0201 — VCC_1V8_S3
PMUIO2 P28 — C1113 100nF X5R 6.3V C0201 — VCC_3V3_S3

RK3588

armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	08.RK3588_OSC/PLL/PMUIO		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 8 of 24

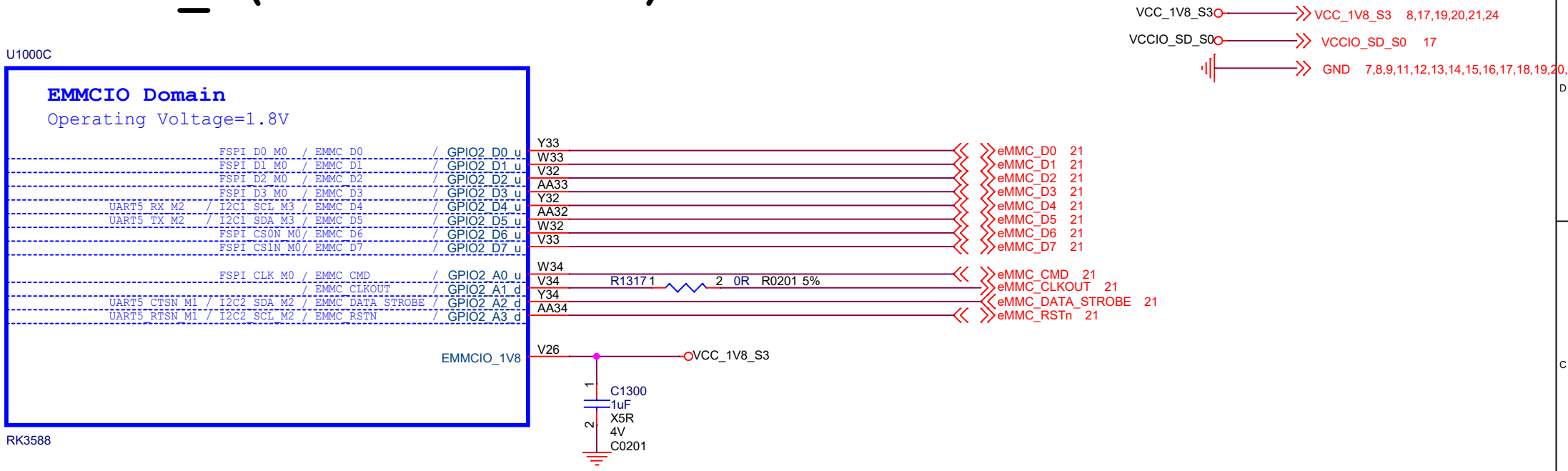


DDR FILTER

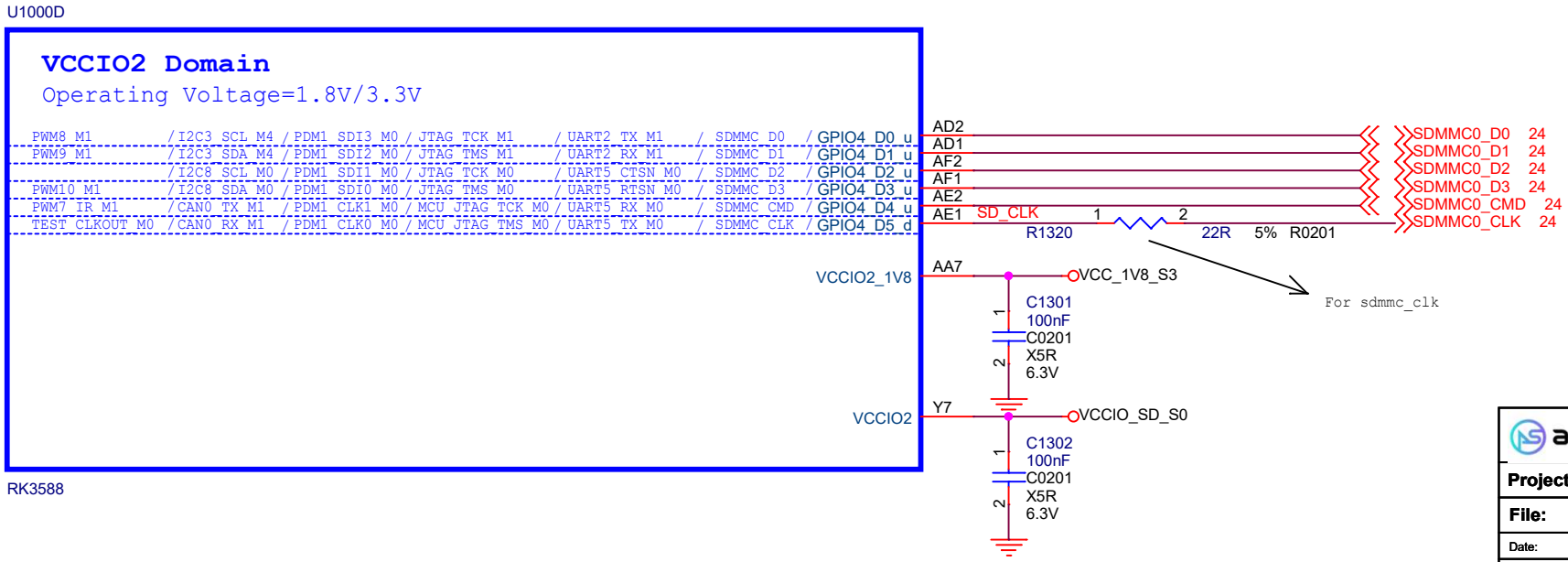


armsom	ArmSoM			
Project:	ArmSoM-AIM7			
File:	09.RK3588 DDR Controler			
Date:	Wednesday, December 20, 2023		Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet:	9 of 24

RK3588_C(EMMCIO Domain)



RK3588_D(VCCIO2 Domain)



armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	10.RK3588_Flash/SD Controller				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	10 of 24

RK3588_M(TYPEC/DP)

U1000M

Note:
If TYPEC0 is not used:
Signal:leave floating
REXT:8.2K ohm 1% resistor must be connected externally
Power: Must supply power

USB3.0 OTG/DP1.4 Alt of TYPEC0

USB:U3/Gen1----Controller0
DP:RBR/HBR/HBR2/HBR3

TYPEC0_SBU1/DP0_AUXP — AL15 — TYPEC0_SBU1/DP0_AUXP 24
TYPEC0_SBU2/DP0_AUXN — AM15 — TYPEC0_SBU2/DP0_AUXN 24
TYPEC0_SSRX1P/DP0_TX0P — AN13 — TYPEC0_SSRX1P/DP0_TX0P 24
TYPEC0_SSRX1N/DP0_TX0N — AP13 — TYPEC0_SSRX1N/DP0_TX0N 24
TYPEC0_SSTX1P/DP0_TX1P — AP14 — TYPEC0_SSTX1P/DP0_TX1P 24
TYPEC0_SSTX1N/DP0_TX1N — AN14 — TYPEC0_SSTX1N/DP0_TX1N 24
TYPEC0_SSRX2P/DP0_TX2P — AN15 — TYPEC0_SSRX2P/DP0_TX2P 24
TYPEC0_SSRX2N/DP0_TX2N — AP15 — TYPEC0_SSRX2N/DP0_TX2N 24
TYPEC0_SSTX2P/DP0_TX3P — AP16 — TYPEC0_SSTX2P/DP0_TX3P 24
TYPEC0_SSTX2N/DP0_TX3N — AN16 — TYPEC0_SSTX2N/DP0_TX3N 24

TYPEC&DP MUX Differential Pair:
DATE:95 Ohm +-10%
USB30 Differential Pair:
DATE:90 Ohm +-10%
DP Differential Pair:
DATE:100 Ohm +-10%

TYPEC0_DP0_REXT — AH16 — TYPEC0_DP0_REXT — R1402 8.2K R0201 1%

TYPEC0_DP0_VDD_0V85 / TYPEC0_DP0_VDDA_0V85 — AJ14 / AH14 — VDDA_0V85_S0
C1400 1uF X5R 6.3V C0201
C1401 100nF X5R 6.3V C0201

Do not delete!!!
For USB30 For DP

TYPEC0_DP0_VDDH_1V8 — AG14 — VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201
C1403 100nF X5R 6.3V C0201

USB3.0 OTG/DP1.4 Alt of TYPEC1

USB:U3/Gen1----Controller1
DP:RBR/HBR/HBR2/HBR3

TYPEC1_SBU1/DP1_AUXP — AL10
TYPEC1_SBU2/DP1_AUXN — AM10
TYPEC1_SSRX1P/DP1_TX0P — AN8
TYPEC1_SSRX1N/DP1_TX0N — AP8
TYPEC1_SSTX1P/DP1_TX1P — AP9
TYPEC1_SSTX1N/DP1_TX1N — AN9
TYPEC1_SSRX2P/DP1_TX2P — AN10
TYPEC1_SSRX2N/DP1_TX2N — AP10
TYPEC1_SSTX2P/DP1_TX3P — AP11
TYPEC1_SSTX2N/DP1_TX3N — AN11

TYPEC1_DP1_REXT — AG16 — TYPEC1_DP1_REXT — R1410 8.2K R0201 1%

TYPEC1_DP1_VDD_0V85 / TYPEC1_DP1_VDDA_0V85 — AH13 / AJ13 — VDDA_0V85_S0
C1404 1uF X5R 6.3V C0201
C1405 100nF X5R 6.3V C0201

TYPEC1_DP1_VDDH_1V8 — AG13 — VCCA_1V8_S0
C1406 1uF X5R 6.3V C0201
C1407 100nF X5R 6.3V C0201

VCCA_1V8_S0 — VCCA_1V8_S0 8,9,12,15,17
GND — 7,8,9,10,12,13,14,15,16,17,18,19,20,21,22,23,24

RK3588

Note:
If need full function of Typec1
(With DP funtion)
please Refer to the circuit of Typec0

If TYPEC1 is not used,
Signal: Leave floating
REXT: Leave floating
Power: Leave floating

USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*USB30 x4Lane*	*TYPEC_SSTX1P/1N&TYPEC_SSRX1P/1N or TYPEC_SSTX2P/2N&TYPEC_SSRX2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:Lane0 Lane1 DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:Lane2 Lane3 DP:Lane0 Lane1*

RK3588_L(USB2.0 HOST/OTG)

U1000L

USB2.0 of TYPEC0 (OTG/HOST/DEVICE)
HS/FS/LS

Download Port

TYPEC0_USB20_OTG_DP — AL12 — TYPEC0_USB20_OTG_DP 24
TYPEC0_USB20_OTG_DM — AM12 — TYPEC0_USB20_OTG_DM 24
TYPEC0_USB20_OTG_ID — AL14 — =1.8V / <=3.3V — R1407 4.7K 5% R0201 — VCCA_3V3_S0
TYPEC0_USB20_VBUSDET — 40K — AM14 — TYPEC0_USB20_VBUSDET 24
TYPEC0_USB20_OTG0_REXT — AP12 — OTG0_REXT — R1405 200R R0201 1%

USB20 Differential Pair:
DATE:90 Ohm +-10%

USB2.0 of TYPEC1 (OTG/HOST/DEVICE)
HS/FS/LS

TYPEC1_USB20_OTG_DP — AK9
TYPEC1_USB20_OTG_DM — AL9
TYPEC1_USB20_OTG_ID — AK8
TYPEC1_USB20_VBUSDET — 40K — AL8
TYPEC1_USB20_OTG1_REXT — AP7 — OTG1_REXT — R1406 200R R0201 1%

USB2.0 HOST0
HS/FS/LS

USB20_HOST0_DP — AK6 — USB20_HOST0_DP 24
USB20_HOST0_DM — AL6 — USB20_HOST0_DM 24
USB20_HOST0_REXT — AG9 — HOST0_REXT — R1400 200R R0201 1%

USB2.0 HOST1
HS/FS/LS

USB20_HOST1_DP — AL7 — USB20_HOST1_DP 24
USB20_HOST1_DM — AM7 — USB20_HOST1_DM 24
USB20_HOST1_REXT — AH9 — HOST1_REXT — R1401 200R R0201 1%

USB2.0 POWER

USB20_DVDD_0V75 — AH10 — VDDA_0V75_S0
C1408 100nF X5R 6.3V C0201

USB20_AVDD_1V8 — AG11 — VCCA_1V8_S0
C1409 100nF X5R 6.3V C0201

USB20_AVDD_3V3 — AJ10 — VCCA_3V3_S0
C1410 100nF X5R 6.3V C0201

RK3588

Note:
TYPEC0_USB20_OTG:
DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

TYPEC1_USB20_OTG:
If not used:
DP/DM:Leave floating
ID:Leave floating
VBUSDET:Leave floating
REXT:Leave floating
Power:Leave floating

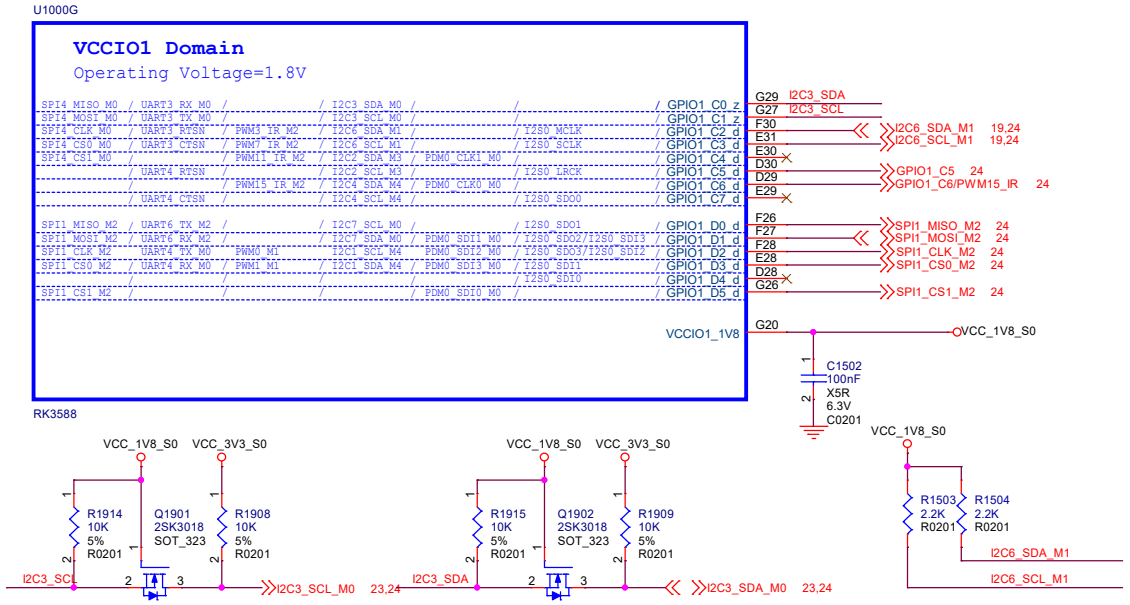
USB20_HOST0/USB20_HOST1:
If not used:
DP/DM:Leave floating
REXT:Leave floating
Power:Leave floating

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 30K ohm resistor.The VBUSDETpin voltage range <=3.3V.

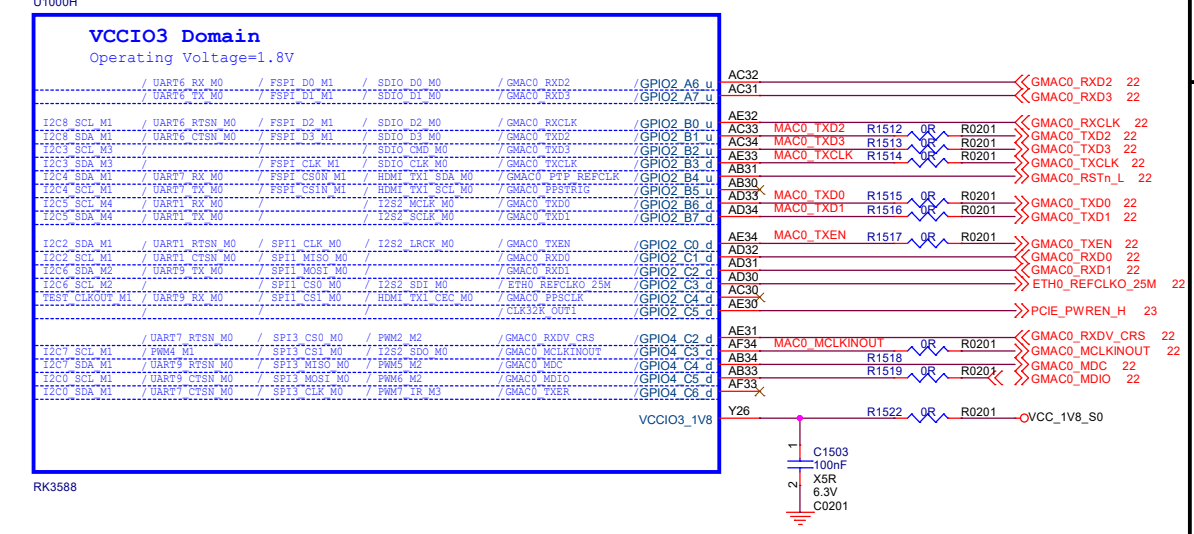
armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	11.RK3588_USB30/USB20_Ctrl				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	11 of 24

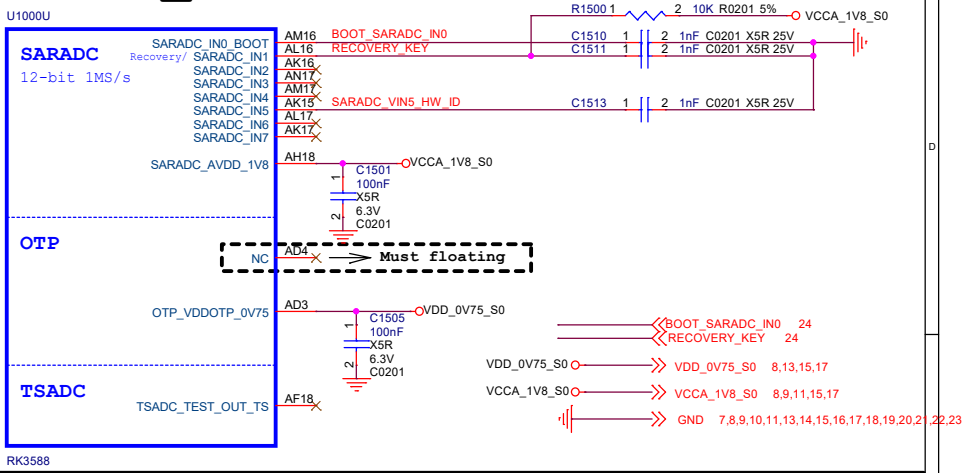
RK3588_G(VCCIO1 Domain)



RK3588_H(VCCIO3 Domain)



RK3588_U(SARADC/OTP)



BOOT MODE CONFIG

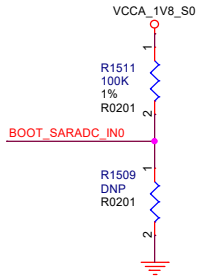


TABLE 1

Item	Rup	Rdown	ADC	VOL	BOOT MODE
LEVEL1	100K	0ohm	0	0V	USB (Maskrom mode)
LEVEL2	100K	20K	682	0.3V	SD Card-USB
LEVEL3	100K	51K	1365	0.6V	EMMC-USB
LEVEL4	100K	100K	2047	0.9V	FSPI M0-USB
LEVEL5	100K	200K	2730	1.2V	FSPI M1-USB
LEVEL6	100K	499K	3412	1.5V	FSPI M2-USB
LEVEL7	100K	DNP	4095	1.8V	FSPI_M2-FSPI_M1-FSPI_M0 -EMMC-SD Card-USB

BOARD ID CONFIG

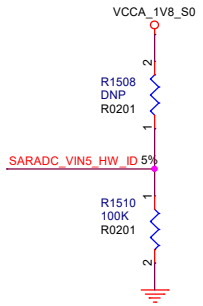


TABLE 2

Item	Rup	Rdown	ADC	VOL	VERSION
LEVEL1	DNP	100K	0	0V	V1.0
LEVEL2	100K	20K	682	0.3V	V2.0
LEVEL3	100K	51K	1365	0.6V	V3.0
LEVEL4	100K	100K	2047	0.9V	V4.0
LEVEL5	100K	200K	2730	1.2V	V5.0
LEVEL6	100K	499K	3412	1.5V	V6.0
LEVEL7	100K	DNP	4095	1.8V	V7.0

armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	12.RK3588_SARADC/1.8V Only GPIO				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	12 of 24

RK3588_Q/R(MIPI_D/C_PHY0/1)

U1000Q

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C — AN26 / AP26 — MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B — AN24 / AP24 — MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A — AN25 / AP25 — MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B — AN27 / AP27 — MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A
MIPI_DPHY0_TX_D3P /NO_USE_AN28 — AN28 / AP28 — MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C

MIPI DPHY Differential Pair: 100 Ohm +-10%

MIPI CPHY Single: 50 Ohm +-10%

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port0

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C — AN32 / AP31 — MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B — MIPI_DPHY0_RX_CLKP 24 / MIPI_DPHY0_RX_CLKN 24
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B — AN29 / AP29 — MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A — MIPI_DPHY0_RX_D0P 24 / MIPI_DPHY0_RX_D0N 24
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A — AN30 / AP30 — MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C — MIPI_DPHY0_RX_D1P 24 / MIPI_DPHY0_RX_D1N 24
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B — AN33 / AP32 — MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A — MIPI_DPHY0_RX_D2P 24 / MIPI_DPHY0_RX_D2N 24
MIPI_DPHY0_RX_D3P /NO_USE_AN34 — AN34 / AP33 — MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C — MIPI_DPHY0_RX_D3P 24 / MIPI_DPHY0_RX_D3N 24

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY0_VREG — AF20 — C1600 1uF — 2 C0201 X5R 4V
MIPI_D/C_PHY0_VDD — AG20 — VDD_0V75_S0
C1602 100nF X5R 6.3V C0201
C1601 1uF X5R 6.3V C0201 — C-PHY 5.7Gbps 0.85V; D-PHY 2.5Gbps & C-PHY 5.7Gbps 0.75V
MIPI_D/C_PHY0_VDD_1V2 — AH20 — VDDA_1V2_S0
C1603 1uF X5R 6.3V C0201
MIPI_D/C_PHY0_VDD_1V8 — AJ20 — VCC_1V8_S0
C1605 1uF X5R 6.3V C0201

RK3588

U1000R

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0 4.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C — AN20 / AP20 — MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B — MIPI_DPHY1_TX_CLKP 24 / MIPI_DPHY1_TX_CLKN 24
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B — AN18 / AP18 — MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A — MIPI_DPHY1_TX_D0P 24 / MIPI_DPHY1_TX_D0N 24
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A — AN19 / AP19 — MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C — MIPI_DPHY1_TX_D1P 24 / MIPI_DPHY1_TX_D1N 24
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B — AN21 / AP21 — MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A
MIPI_DPHY1_TX_D3P /NO_USE_AN22 — AN22 / AP22 — MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C

TX and RX port must work in the same mode, DPHY or CPHY

MIPI D/C-PHY CSI_RX Port1

D-PHY:V1.2 2.5Gbps/Lane
C-PHY:V1.1 5.7Gbps/Trio

Note:
此D-PHY使用受限!!!
详细情况请参阅硬件设计指南。
This D-PHY is limited!!!
Please refer to the hardware design guide for details.

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C — AK20 / AL20 — MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B — AK18 / AL18 — MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A — AK19 / AL19 — MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B — AK21 / AL21 — MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A
MIPI_DPHY1_RX_D3P /NO_USE_AK22 — AK22 / AL22 — MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C

Note:
Suggest Using 1/2 lane mode, Using 4Lane is limited, Please refer to the hardware design guide for details.

MIPI D/C-PHY POWER

MIPI_D/C_PHY1_VREG — AF19 — C1608 1uF — 2 C0201 X5R 4V
MIPI_D/C_PHY1_VDD — AG19 — VDD_0V75_S0
C1609 1uF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V2 — AH19 — VDDA_1V2_S0
C1611 100nF X5R 6.3V C0201
MIPI_D/C_PHY1_VDD_1V8 — AJ19 — VCC_1V8_S0
C1613 1uF X5R 6.3V C0201

Note:
If not used:
Signal:leave floating
Power: Floating

RK3588

RK3588_P(MIPI_DPHY_CSI_RX_PHY)

U1000P

MIPI DPHY CSI_RX Port0

MIPI V1.2/2.5Gbps

MIPI_CSI0_CLK0P/MIPI_CSI0_CLK0N — AJ33 / AJ34 — MIPI_CSI0_RX_CLK0P 24 / MIPI_CSI0_RX_CLK0N 24
MIPI_CSI0_D0P/MIPI_CSI0_D0N — AG33 / AG34 — MIPI_CSI0_RX_D0P 24 / MIPI_CSI0_RX_D0N 24
MIPI_CSI0_D1P/MIPI_CSI0_D1N — AH33 / AH34 — MIPI_CSI0_RX_D1P 24 / MIPI_CSI0_RX_D1N 24
MIPI_CSI0_CLK1P/MIPI_CSI0_CLK1N — AM33 / AM34 — MIPI_CSI0_RX_CLK1P 24 / MIPI_CSI0_RX_CLK1N 24
MIPI_CSI0_D2P/MIPI_CSI0_D2N — AK33 / AK34 — MIPI_CSI0_RX_D2P 24 / MIPI_CSI0_RX_D2N 24
MIPI_CSI0_D3P/MIPI_CSI0_D3N — AL33 / AL34 — MIPI_CSI0_RX_D3P 24 / MIPI_CSI0_RX_D3N 24

MIPI CSI Differential Pair: 100 Ohm +-10%

MIPI_CSI0_AVCC0V75 — AB25 — VDD_0V75_S0
C1616 100nF X5R 6.3V C0201
C1615 1uF X5R 6.3V C0201
MIPI_CSI0_AVCC1V8 — AB26 — VCC_1V8_S0
C1617 1uF X5R 6.3V C0201

MIPI DPHY CSI_RX Port1

MIPI V1.2/2.5Gbps

MIPI_CSI1_CLK0P/MIPI_CSI1_CLK0N — AJ31 / AJ32 — MIPI_CSI1_RX_CLK0P 24 / MIPI_CSI1_RX_CLK0N 24
MIPI_CSI1_D0P/MIPI_CSI1_D0N — AG31 / AG32 — MIPI_CSI1_RX_D0P 24 / MIPI_CSI1_RX_D0N 24
MIPI_CSI1_D1P/MIPI_CSI1_D1N — AH31 / AH32 — MIPI_CSI1_RX_D1P 24 / MIPI_CSI1_RX_D1N 24
MIPI_CSI1_CLK1P/MIPI_CSI1_CLK1N — AM31 / AM32 — MIPI_CSI1_RX_CLK1P 24 / MIPI_CSI1_RX_CLK1N 24
MIPI_CSI1_D2P/MIPI_CSI1_D2N — AK31 / AK32 — MIPI_CSI1_RX_D2P 24 / MIPI_CSI1_RX_D2N 24
MIPI_CSI1_D3P/MIPI_CSI1_D3N — AL31 / AL32 — MIPI_CSI1_RX_D3P 24 / MIPI_CSI1_RX_D3N 24

MIPI_CSI1_AVCC0V75 — AA25 — VDD_0V75_S0
C1619 1uF X5R 6.3V C0201
MIPI_CSI1_AVCC1V8 — AA26 — VCC_1V8_S0
C1621 100nF X5R 6.3V C0201

RK3588

Note:
建义优先使用U1000P这个模块的DPHY CSI_RX。
First use the DPHY_CSI_RX controller of U1000P.

MIPI_CSI_RX Configuration

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* + *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0*
		MIPI_CSI_RX_D2-3 *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lanel is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lanel,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

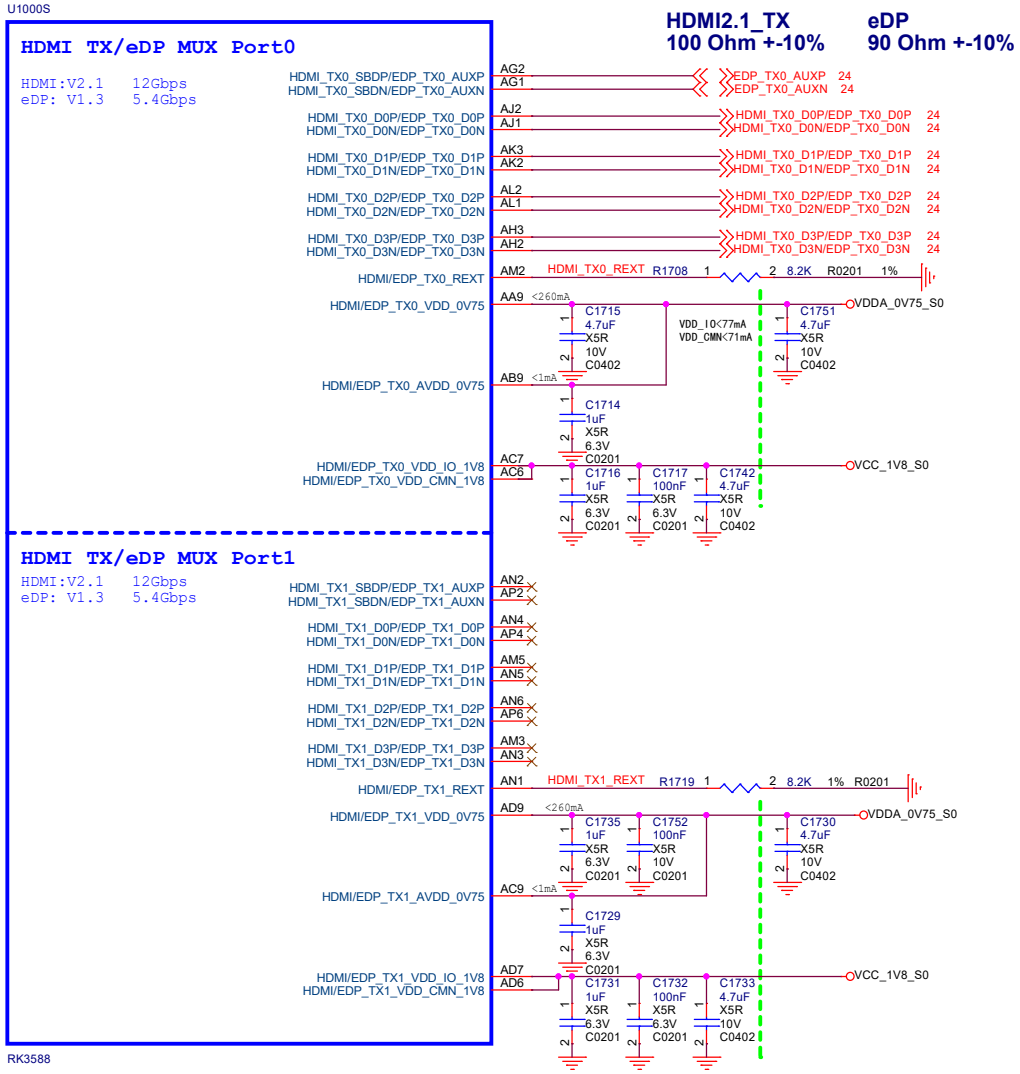
Note:
If not used:
Signal:leave floating
Power: Floating

VDD_0V75_S0 → VDD_0V75_S0 8,12,15,17
GND 7,8,9,10,11,12,14,15,16,17,18,19,20,21,22,23,24

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	13.RK3588_MIPI Interface				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	13 of 24

RK3588_S(HDMI2.1 TX)

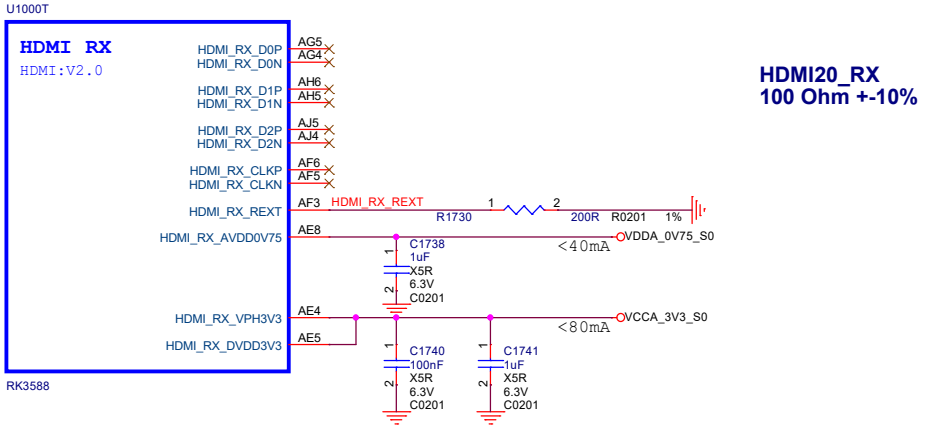
Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.



Note:
The Caps to the left of green line should be placed under the U1000 package.Other caps should be placed close to the U1000 package.

Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

RK3588_T(HDMI20 RX)



Note:
If not used:
Signal:leave floating
Power: Floating

GND 7,8,9,10,11,12,13,15,16,17,18,19,20,21,22,23,24

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	14.RK3588_HDMI/eDP Interface				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	14 of 24

RK3588_N(PCIE20)

U1000N

PCIE20/SATA30 Mux0

PCIe20x1_2 1Lane(RC)--4(1L2)

SATA30 HOST Controller0

MUX

input or output

PCIE20_0_REFCLKP / PCIE20_0_REFCLKN — L32 / L33 — PCIE20_0_REFCLKP 24 / PCIE20_0_REFCLKN 24

PCIE20_0_TXP/SATA30_0_TXP / PCIE20_0_TXN/SATA30_0_TXN — M34 / M33 — PCIE20_0_TXP/SATA30_0_TXP 24 / PCIE20_0_TXN/SATA30_0_TXN 24

PCIE20_0_RXP/SATA30_0_RXP / PCIE20_0_RXN/SATA30_0_RXN — N33 / N34 — PCIE20_0_RXP/SATA30_0_RXP 24 / PCIE20_0_RXN/SATA30_0_RXN 24

PCIE20_SATA30_0_AVDD_0V85 — M28 — C1810 10uF X5R 4V C0402 — VDDA_0V85_S0

PCIE20_SATA30_0_AVDD_1V8 — M27 — C1808 1uF X5R 4V C0201 — VCCA_1V8_S0

CLK Differential Pair: 100 Ohm±10%
DATA Differential Pair: PCIE20: 85 Ohm ±10% SATA30: 100 Ohm ±10% USB30: 90ohm ±10%

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30 Mux1

PCIe30x1_0 1Lane(RC)--2(1L0)

SATA30 HOST Controller1

MUX

input or output

PCIE20_1_REFCLKP / PCIE20_1_REFCLKN — H32 / H33

PCIE20_1_TXP/SATA30_1_TXP / PCIE20_1_TXN/SATA30_1_TXN — K33 / K34

PCIE20_1_RXP/SATA30_1_RXP / PCIE20_1_RXN/SATA30_1_RXN — J33 / J34

PCIE20_SATA30_1_AVDD_0V85 — L28 — C1818 100nF X5R 6.3V C0201 — VDDA_0V85_S0

PCIE20_SATA30_1_AVDD_1V8 — L27 — C1816 100nF X5R 6.3V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
SATA30:Gen1/Gen2/Gen3

PCIE20/SATA30/USB30 HOST Mux2

PCIe30x1_1 1Lane(RC)--3(1L1)

SATA30 HOST Controller2

USB30 HOST Controller2

MUX

input or output

PCIE20_2_REFCLKP / PCIE20_2_REFCLKN — G31 / G30

PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN — H30 / H29 — PCIE20_2_TXP/SATA30_2_TXP/USB30_2_SSTXP 24 / PCIE20_2_TXN/SATA30_2_TXN/USB30_2_SSTXN 24

PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN — J31 / J30 — PCIE20_2_RXP/SATA30_2_RXP/USB30_2_SSRXP 24 / PCIE20_2_RXN/SATA30_2_RXN/USB30_2_SSRXN 24

PCIE20_SATA30_USB30_2_AVDD_0V85 — K28 — C1806 1uF X5R 4V C0201 — VDDA_0V85_S0

PCIE20_SATA30_USB30_2_AVDD_1V8 — K27 — C1804 1uF X5R 4V C0201 — VCCA_1V8_S0

PCIE20:Gen1/Gen2
USB 30:Gen1
SATA30:Gen1/Gen2/Gen3

RK3588

Note:
If not used:
Signal:leave floating
Power: Floating

Note:
The SATA differential trace impedance is 100 OHM
The SATA trace length is less than 5 inch

VDD_0V75_S0 — VDD_0V75_S0 8,12,13,17

VCCA_1V8_S0 — VCCA_1V8_S0 8,9,11,12,17

GND 7,8,9,10,11,12,13,14,16,17,18,19,20,21,22,23,24

RK3588_O(PCIE30)

Note:
Only PCIE3.0 Controller 0 support RC and EP,Other controller only support RC Mode.

U1000O

PCIE30X4

PCIe30X4 4Lane(DM)--0(4L)

PCIe30x1_0 1Lane(RC)--2(1L0) — PCIE20/SATA30 MUX1

PCIe30x2 2Lane(RC)--1(2L)

PCIe30x1_1 1Lane(RC)--3(1L1) — PCIE20/SATA30/USB30 MUX2

PCIE30:
PCIe1.1(2.5Gbps)
PCIe2.1(5Gbps)
PCIe3.0(8Gbps)

PCIE30 PORT0

input PCIE30_PORT0_REF_CLKP / PCIE30_PORT0_REF_CLKN — E33 / E34 — PCIE30_PORT0_REFCLKP_IN 23 / PCIE30_PORT0_REFCLKN_IN 23

Lane0

PCIE30_PORT0_TX0P / PCIE30_PORT0_TX0N — D32 / D33 — PCIE30_PORT0_TX0P 24 / PCIE30_PORT0_TX0N 24

PCIE30_PORT0_RX0P / PCIE30_PORT0_RX0N — G33 / G34 — PCIE30_PORT0_RX0P 24 / PCIE30_PORT0_RX0N 24

Lane1

PCIE30_PORT0_TX1P / PCIE30_PORT0_TX1N — C33 / C34 — PCIE30_PORT0_TX1P 24 / PCIE30_PORT0_TX1N 24

PCIE30_PORT0_RX1P / PCIE30_PORT0_RX1N — F32 / F33 — PCIE30_PORT0_RX1P 24 / PCIE30_PORT0_RX1N 24

PCIE30_PORT0_RESREF — B34 — PCIE30_0_REF — R1801 1 2 200R 1% R0201

PCIE30_PORT0_AVDD0V75 — G24 — VDD_0V75_S0
C1802 1uF X5R 6.3V C0201
C1803 4.7uF X5R 10V C0402

PCIE30_PORT0_AVDD1V8 — G23 — VCCA_1V8_S0
C1800 1uF X5R 6.3V C0201
C1801 4.7uF X5R 10V C0402

PCIE30 PORT1

input PCIE30_PORT1_REF_CLKP / PCIE30_PORT1_REF_CLKN — A28 / B28 — PCIE30_PORT1_REFCLKP_IN 23 / PCIE30_PORT1_REFCLKN_IN 23

Lane0

PCIE30_PORT1_TX0P / PCIE30_PORT1_TX0N — B30 / A30 — PCIE30_PORT1_TX2P 24 / PCIE30_PORT1_TX2N 24

PCIE30_PORT1_RX0P / PCIE30_PORT1_RX0N — B32 / A32 — PCIE30_PORT1_RX2P 24 / PCIE30_PORT1_RX2N 24

Lane1

PCIE30_PORT1_TX1P / PCIE30_PORT1_TX1N — C29 / B29 — PCIE30_PORT1_TX3P 24 / PCIE30_PORT1_TX3N 24

PCIE30_PORT1_RX1P / PCIE30_PORT1_RX1N — C31 / B31 — PCIE30_PORT1_RX3P 24 / PCIE30_PORT1_RX3N 24

PCIE30_PORT1_RESREF — A33 — PCIE30_1_REF — R1807 1 2 200R 1% R0201

PCIE30_PORT1_AVDD0V75 — H24 — VDD_0V75_S0
C1814 1uF X5R 6.3V C0201
C1815 4.7uF X5R C0402 10V

PCIE30_PORT1_AVDD1V8 — H23 — VCCA_1V8_S0
C1812 100nF X5R 6.3V C0201
C1813 4.7uF X5R 10V C0402

CLK Differential Pair: 100 Ohm ±10%

DATA Differential Pair: PCIE30: 85 Ohm ±10%

RK3588

Note:

If Port0 and Port1 are not used,
Port0 and Port1 REF_CLKP/N: Leave floating or tie to VSS
Port0 and Port1 Other Signal: Leave floating
Port0 and Port1 Power: Leave floating or tie to VSS

If Port0 is used ,Port1 is not used,
Port1 REF_CLKP/N: Leave floating or tie to VSS
Port1 Other Signal: Leave floating
Port1 Power: Must supply power

If Port1 is used ,Port0 is not used,
Port0 REF_CLKP/N: Leave floating or tie to VSS
Port0 Other Signal: Leave floating
Port0 Power: Must supply power

armsom ArmSoM

Project:	ArmSoM-AIM7				
File:	15.RK3588_PCIE30/PCIE20/SATA30				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	15 of 24

RK3588_J(VCCIO5 Domain)

U1000J

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

PWM10_M0	SPI4_MISO_M1		I2C6_SDA_M4	FSPI_D0_M2	I2S3_MCLK	SDIO_D0_M1	GMAC1_TXD2	GPIO3_A0_u	AA29
AUDDSM_LN	SPI4_MOSI_M1	PWM11_IR_M0	I2C6_SCL_M4	FSPI_D1_M2	I2S3_SCLK	SDIO_D1_M1	GMAC1_TXD3	GPIO3_A1_u	AA30
AUDDSM_LP	SPI4_CLK_M1	UART8_TX_M1		FSPI_D2_M2	I2S3_LRCK	SDIO_D2_M1	GMAC1_RXD2	GPIO3_A2_u	AD27
AUDDSM_RN	SPI4_CS0_M1	UART8_RX_M1		FSPI_D3_M2	I2S3_SDO	SDIO_D3_M1	GMAC1_RXD3	GPIO3_A3_u	AE27
AUDDSM_RP	SPI4_CS1_M1	UART8_RTSN_M1			I2S3_SDI	SDIO_CMD_M1	GMAC1_TXCLK	GPIO3_A4_d	AD28
	MIPI_CAMERA0_CLK_M1	UART8_CTSN_M1	I2C4_SDA_M0	FSPI_CLK_M2		SDIO_CLK_M1	GMAC1_RXCLK	GPIO3_A5_d	AH30
	MIPI_CAMERA1_CLK_M1		I2C4_SCL_M0				ETH1_REFCLKO_25M	GPIO3_A6_d	AH27
PWM8_M0	MIPI_CAMERA2_CLK_M1						GMAC1_RXD0	GPIO3_A7_u	AG29
PWM9_M0	MIPI_CAMERA3_CLK_M1						GMAC1_RXD1	GPIO3_B0_u	AG28
PWM2_M1	MIPI_CAMERA4_CLK_M1	UART2_TX_M2					GMAC1_RXDV_CRS	GPIO3_B1_d	AH29
PWM3_IR_M1		UART2_RX_M2			I2S2_SDI_M1		GMAC1_TXER	GPIO3_B2_d	AE28
		UART2_RTSN			I2S2_SDO_M1		GMAC1_TXD0	GPIO3_B3_u	AC28
		UART2_CTSN			I2S2_MCLK_M1		GMAC1_TXD1	GPIO3_B4_u	AC29
PWM12_M0	CAN1_RX_M0	UART3_TX_M1			I2S2_SCLK_M1		GMAC1_TXEN	GPIO3_B5_u	AD29
PWM13_M0	CAN1_TX_M0	UART3_RX_M1			I2S2_LRCK_M1		GMAC1_MCLKINOUT	GPIO3_B6_d	AE29
			I2C3_SCL_M1	SPI1_MOSI_M1	HDMI_TX1_HPD_M1		GMAC1_PTP_REF_CLK	GPIO3_B7_d	AA28
		UART7_TX_M1	I2C3_SDA_M1	SPI1_MISO_M1			GMAC1_PPSTRIG	GPIO3_C0_d	Y29
	PCIE30X2_BUTTON_RSTN	UART7_RX_M1		SPI1_CLK_M1			GMAC1_PPSCLK	GPIO3_C1_d	Y27
PWM14_M0		UART7_RTSN_M1	I2C8_SCL_M4	SPI1_CS0_M1		MIPI_TE0	GMAC1_MDC	GPIO3_C2_d	Y31
PWM15_IR_M0		UART7_CTSN_M1	I2C8_SDA_M4	SPI1_CS1_M1		MIPI_TE1	GMAC1_MDIO	GPIO3_C3_d	Y30
CAN2_RX_M0	PCIE30X4_CLKREQN_M2	UART5_TX_M1	FSPI_CS0N_M2	SPI3_CS0_M3	HDMI_TX1_CEC_M2		CIF_D8	GPIO3_C4_u	AH26
CAN2_TX_M0	PCIE30X4_WAKEN_M2	UART5_RX_M1	FSPI_CS1N_M2	SPI3_CS1_M3	HDMI_TX1_SDA_M1		CIF_D9	GPIO3_C5_u	AH25
	PCIE30X4_PERSTN_M2			SPI3_MISO_M3	HDMI_TX1_SCL_M1		CIF_D10	GPIO3_C6_u	AG26
	PCIE20X1_2_CLKREQN_M0		I2C5_SCL_M0	SPI3_MOSI_M3	HDMI_TX0_SCL_M2		CIF_D11	GPIO3_C7_u	AJ24
PWM8_M2	PCIE20X1_2_WAKEN_M0	UART4_RX_M1	I2C5_SDA_M0	SPI3_CLK_M3	HDMI_TX0_SDA_M2		CIF_D12	GPIO3_D0_u	AH24
PWM9_M2	PCIE20X1_2_PERSTN_M0	UART4_TX_M1		SPI0_MISO_M3	HDMI_RX_CEC_M1		CIF_D13	GPIO3_D1_d	AG23
	PCIE30X2_CLKREQN_M2	UART9_RTSN_M2	I2C7_SCL_M2	SPI0_MOSI_M3	HDMI_RX_SCL_M1		CIF_D14	GPIO3_D2_d	AG25
PWM10_M2	PCIE30X2_WAKEN_M2	UART9_CTSN_M2	I2C7_SDA_M2	SPI0_CLK_M3	HDMI_RX_SDA_M1		CIF_D15	GPIO3_D3_d	AG24
	PCIE30X2_PERSTN_M2	UART9_RX_M2		SPI0_CS0_M3	HDMI_RX_HPDOUT_M1/	HDMI_TX0_HPD_M1/	MCU_JTAG_TCK_M1	GPIO3_D4_d	AA27
PWM11_IR_M3	PCIE30X4_BUTTON_RSTN	UART9_TX_M2		SPI0_CS1_M3	DP1_HPDIN_M0		MCU_JTAG_TMS_M1	GPIO3_D5_d	AB28

VCCIO5_1V8 — W25 — C1903 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO5 — W26 — C1902 100nF X5R 6.3V C0201 — VCC_1V8_S0

AJ24 PCIE20X1_2_CLKREQN

AG23 PCIE20X1_2_PERSTN

RK3588

RK3588_K(VCCIO6 Domain)

U1000K

VCCIO6 Domain

Operating Voltage=1.8V/3.3V

	SPI0_MISO_M1	UART9_RTSN_M1 /			I2S1_MCLK_M0	PCIE30X1_1_CLKREQN_M1	BT1120_D0	CIF_D0	GPIO4_A0_d	AK30
	SPI0_MOSI_M1	UART9_CTSN_M1 /			I2S1_SCLK_M0	PCIE30X1_1_WAKEN_M1	BT1120_D1	CIF_D1	GPIO4_A1_d	AL30
	SPI0_CLK_M1	/			I2S1_LRCK_M0	PCIE30X1_1_PERSTN_M1	BT1120_D2	CIF_D2	GPIO4_A2_d	AM29
	/	UART0_TX_M2	/		/	PCIE30X1_0_CLKREQN_M1	BT1120_D3	CIF_D3	GPIO4_A3_d	AL29
	SPI2_MISO_M1	UART0_RX_M2	I2C3_SCL_M2		/	PCIE30X1_0_WAKEN_M1	BT1120_D4	CIF_D4	GPIO4_A4_d	AL28
	SPI2_MOSI_M1	UART3_TX_M2	I2C3_SDA_M2		I2S1_SDI0_M0	PCIE30X1_0_PERSTN_M1	BT1120_D5	CIF_D5	GPIO4_A5_d	AK27
	SPI2_CLK_M1	UART3_RX_M2	I2C5_SCL_M2		I2S1_SDI1_M0	PCIE30X2_CLKREQN_M1	BT1120_D6	CIF_D6	GPIO4_A6_d	AL27
	SPI2_CS0_M1	/	I2C5_SDA_M2		I2S1_SDI2_M0	PCIE30X2_WAKEN_M1	BT1120_D7	CIF_D7	GPIO4_A7_d	AM27
	SPI2_CS1_M1	UART8_TX_M0	I2C6_SDA_M3		I2S1_SDI3_M0	PCIE30X2_PERSTN_M1	BT1120_CLKOUT	CIF_CLKIN	GPIO4_B0_d	AK26
SATA2_ACT_LED_M0	SPDIF1_TX_M1	SPI0_CS1_M1	UART8_RX_M0	I2C6_SCL_M3		I2S1_SDO0_M0	PCIE30X1_0_BUTTON_RSTN	/	MIPI_CAMERA0_CLK_M0 /	GPIO4_B1_u	AL24
CAN1_RX_M1	PWM14_M1	SPI0_CS0_M1	UART8_RTSN_M0	I2C7_SCL_M3		I2S1_SDO1_M0	PCIE30X1_1_BUTTON_RSTN	BT1120_D8	CIF_HREF	GPIO4_B2_u	AK25
CAN1_TX_M1	PWM15_IR_M1	/	UART8_CTSN_M0	I2C7_SDA_M3		I2S1_SDO2_M0	PCIE20X1_2_BUTTON_RSTN	BT1120_D9	CIF_VSYNC	GPIO4_B3_u	AM25
SPDIF0_TX_M1	PWM11_IR_M1	DP0_HPDIN_M0	UART9_TX_M1			I2S1_SDO3_M0	PCIE30X4_CLKREQN_M1	BT1120_D10	CIF_CLKOUT	GPIO4_B4_u	AL26
SATA1_ACT_LED_M0	PWM12_M1	SPI3_MISO_M1	UART9_RX_M1	/		HDMI_RX_CEC_M0	PCIE30X4_WAKEN_M1	BT1120_D11	/	GPIO4_B5_d	AJ26
SATA0_ACT_LED_M0	PWM13_M1	SPI3_MOSI_M1	/		I2C5_SCL_M1	HDMI_RX_HPDOUT_M0 /	PCIE30X4_PERSTN_M1	BT1120_D12	/	GPIO4_B6_d	AJ27
	/	SPI3_CLK_M1	/		I2C5_SDA_M1	HDMI_TX0_SCL_M0	PCIE20X1_2_CLKREQN_M1	BT1120_D13	/	GPIO4_B7_u	AJ28
	/	SPI3_CS0_M1	/		I2C8_SCL_M3	HDMI_TX0_SDA_M0	PCIE20X1_2_WAKEN_M1	BT1120_D14	/	GPIO4_C0_u	AJ25
SPDIF1_TX_M2	PWM6_M1	SPI3_CS1_M1	/		I2C8_SDA_M3	HDMI_TX0_CEC_M0	PCIE20X1_2_PERSTN_M1	BT1120_D15	/	GPIO4_C1_d	AK24

VCCIO6_1V8 — AC25 — C1909 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO6 — AC26 — C1908 100nF X5R 6.3V C0201 — VCC_1V8_S0

AK30 GPIO4_A0/I2S1_MCLK_M0/PCIE30X1_1_CLKREQN

AL30 I2S1_SCLK_M0/PCIE30X1_1_WAKEN_M1

AM29 I2S1_LRCK_M0/PCIE30X1_1_PERSTN_M1

AL29 GPIO4_A3/PCIE30X1_0_CLKREQN_M1

AL28 GPIO4_A4/PCIE30X1_0_WAKEN_M1

AK27 I2S1_SDI0_M0/PCIE30X1_0_PERSTN_M1

AL27 MIPI_CAM1_PDN/PCIE30X2_CLKREQN_M1

AM27 GPIO4_A7/PCIE30X2_WAKEN_M1

AK26 GPIO4_B0/PCIE30X2_PERSTN_M1

AL24 I2S1_SDO0_M0

AJ28 HDMI_TX0_SCL_M0

AJ25 HDMI_TX0_SDA_M0

AK24 HDMI_TX0_CEC_M0

RK3588

RK3588_I(VCCIO4 Domain)

U1000I

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

		SPI4_MISO_M2	PCIE30X1_1_CLKREQN_M2/	DP0_HPDIN_M2		I2C2_SDA_M4	UART6_RX_M1	GPIO1_A0_d	A24
SATA1_ACT_LED_M1	/	SPI4_MOSI_M2	PCIE30X1_1_WAKEN_M2	DP1_HPDIN_M2		I2C2_SCL_M4	UART6_TX_M1	GPIO1_A1_d	A25
	PWM0_M2	SPI4_CLK_M2	/		VOP_POST_EMPTY	I2C4_SDA_M3	UART6_RTSN_M1	GPIO1_A2_d	A26
	PWM1_M2	SPI4_CS0_M2	/		HDMI_TX1_SDA_M2	I2C4_SCL_M3	UART6_CTSN_M1	GPIO1_A3_d	A27
	/	SPI2_MISO_M0	/		HDMI_TX1_SCL_M2	/	/	GPIO1_A4_d	B25
	/	SPI2_MOSI_M0			HDMI_TX0_HPD_M0	/	/	GPIO1_A5_d	B26
	/	SPI2_CLK_M0	/		HDMI_TX1_HPD_M0	/	/	GPIO1_A6_d	C24
	PWM3_IR_M3	SPI2_CS0_M0	PCIE30X1_1_PERSTN_M2	/		PDM1_SDI0_M1	/	GPIO1_A7_u	C25
	/	SPI2_CS1_M0	PCIE30X4_CLKREQN_M3	/		PDM1_SDI1_M1	/	GPIO1_B0_u	C27
	/	SPI0_MISO_M2	PCIE30X4_WAKEN_M3	/		PDM1_SDI2_M1	/	GPIO1_B1_d	D25
	/	SPI0_MOSI_M2	PCIE30X4_PERSTN_M3	/		PDM1_SDI3_M1	UART4_RX_M2	GPIO1_B2_d	D26
SATA0_ACT_LED_M1	/	SPI0_CLK_M2	PCIE30X1_0_WAKEN_M2	/		PDM1_CLK1_M1	UART4_TX_M2	GPIO1_B3_d	D27
	/	SPI0_CS0_M2	PCIE30X1_0_PERSTN_M2	/		PDM1_CLK0_M1	UART7_RX_M2	GPIO1_B4_u	E24
	/	SPI0_CS1_M2	PCIE30X1_0_CLKREQN_M2/			/	UART7_TX_M2	GPIO1_B5_u	E25
HDMI_RX_HPDOUT_M2/		SPDIF0_TX_M0	PCIE30X2_WAKEN_M3	MIPI_CAMERA1_CLK_M0 /		I2C5_SCL_M3	UART1_TX_M1	GPIO1_B6_u	E26
SATA2_ACT_LED_M1/	HDMI_RX_CEC_M2	PWM13_M2	SPDIF1_TX_M0	PCIE30X2_PERSTN_M3	MIPI_CAMERA2_CLK_M0 /	I2C5_SDA_M3	UART1_RX_M1	GPIO1_B7_u	E27
HDMI_RX_SCL_M2	/	PWM14_M2	/	/	MIPI_CAMERA3_CLK_M0 /	I2C8_SCL_M2	UART1_RTSN_M1	GPIO1_D6_u	F24
HDMI_RX_SDA_M2	/	PWM15_IR_M3 /		PCIE30X2_CLKREQN_M3	/ MIPI_CAMERA4_CLK_M0 /	I2C8_SDA_M2	UART1_CTSN_M1	GPIO1_D7_u	F25

VCCIO4_1V8 — H20 — C1907 100nF X5R 6.3V C0201 — VCC_1V8_S0

VCCIO4 — H21 — C1906 100nF X5R 6.3V C0201 — VCC_1V8_S0

A24 DP0_HPDIN_M2

B26 HDMI_TX0_HPD_M0

D25 SPI0_MISO_M2

D26 SPI0_MOSI_M2

D27 SPI0_CLK_M2

E24 SPI0_CS0_M2

E25 SPI0_CS1_M2

E26 UART1_TX_M1

E27 UART1_RX_M1

F24 UART1_RTSn_M1

F25 UART1_CTSn_M1

RK3588

VCC_1V8_S0 VCC_3V3_S0

R1916 10K 5% R0201 — Q1903 2SK3018 SOT_323 — R1917 10K 5% R0201

PCIE20X1_2_CLKREQN — PCIE20X1_2_CLKREQN_M0 24

VCC_1V8_S0 VCC_3V3_S0

R1918 10K 5% R0201 — Q1904 2SK3018 SOT_323 — R1919 10K 5% R0201

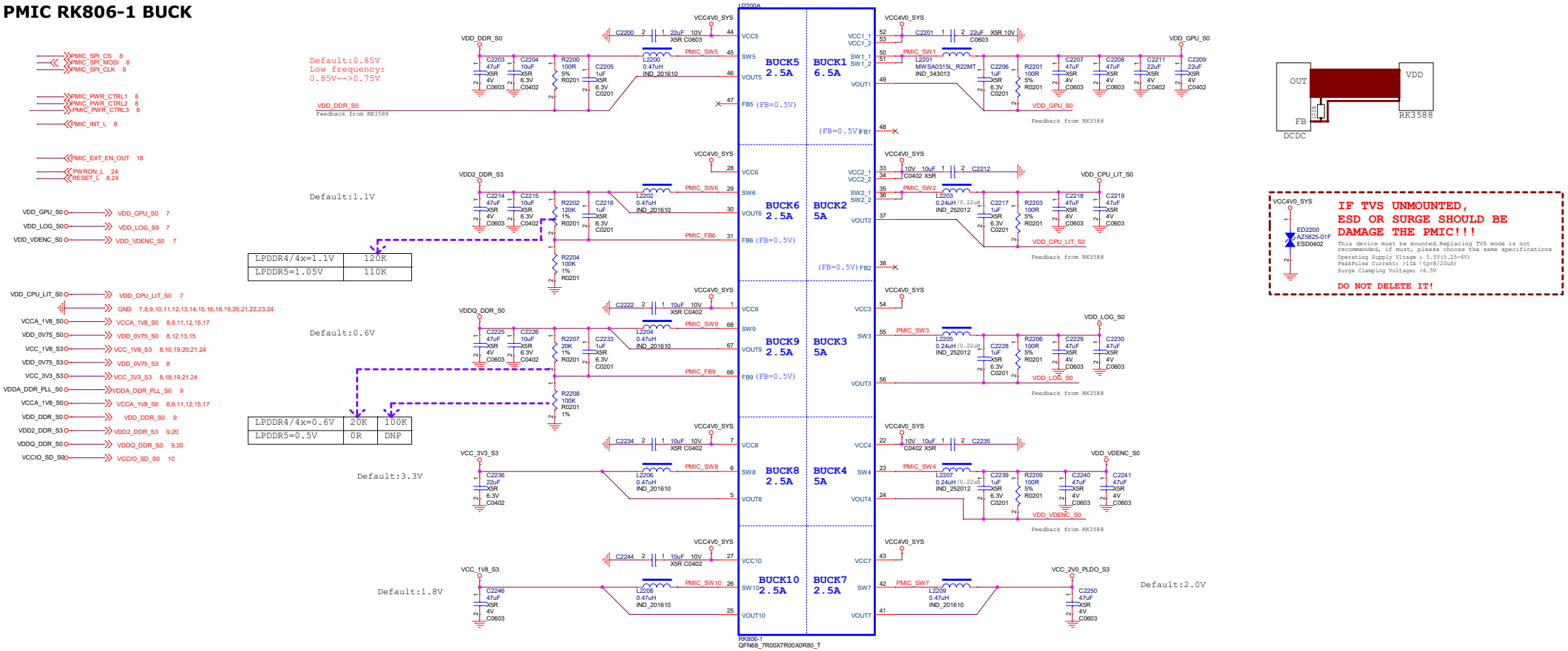
PCIE20X1_2_PERSTN — PCIE20X1_2_PERSTN_M0 24

GND 7,8,9,10,11,12,13,14,15,17,18,19,20,21,22,23,24

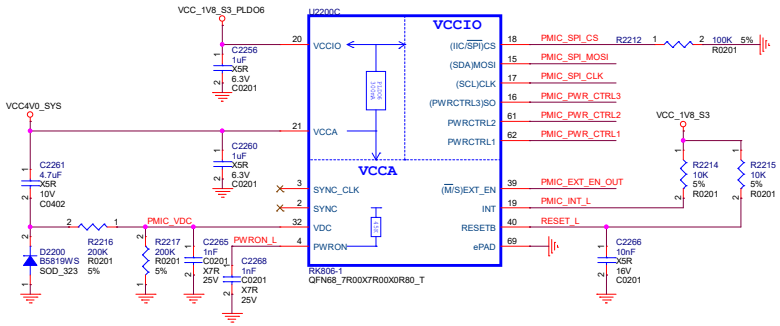
armsom ArmSoM

Project:	ArmSoM-AIM7		
File:	16.RK3588_1.8V/ 3.3V GPIO		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
Designed by: Liu Xinglin	Reviewed by: <Checker>	Sheet:	16 of 24

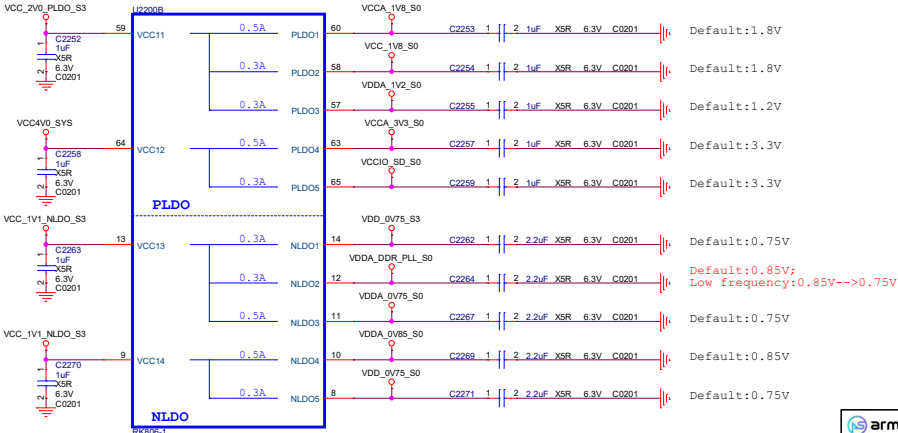
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment

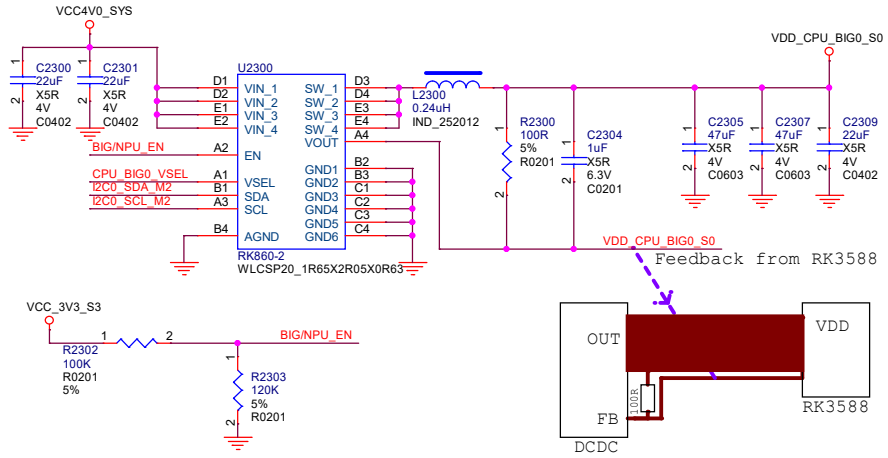


PMIC RK806-1 LDO

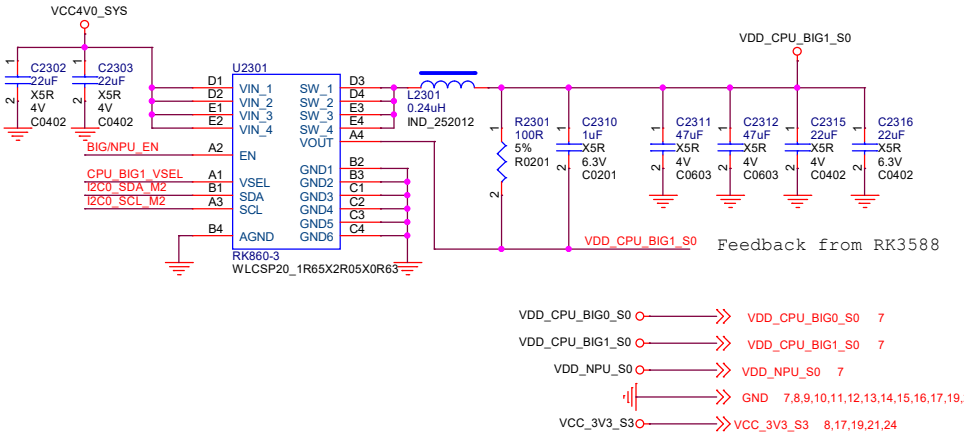


armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	17.Power-PMIC_RK806-1		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 17 of 24

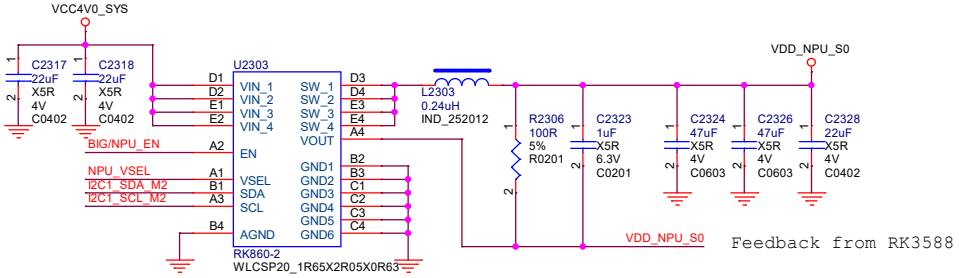
VDD_CPU_BIG0



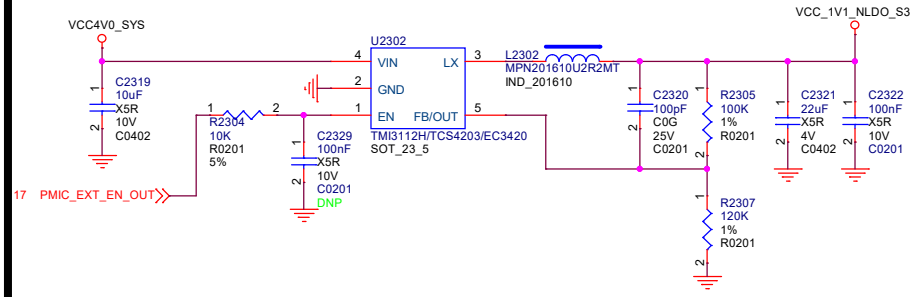
VDD_CPU_BIG1

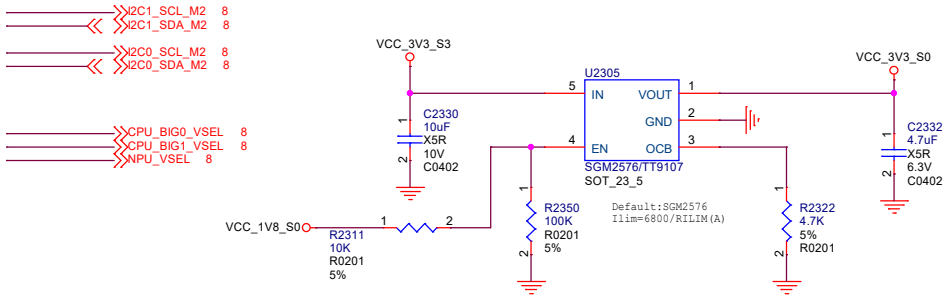


VDD_NPU

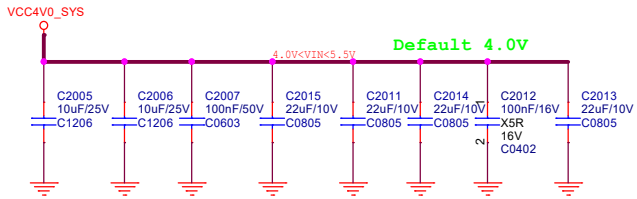


VCC_1V1_NLDO_S3



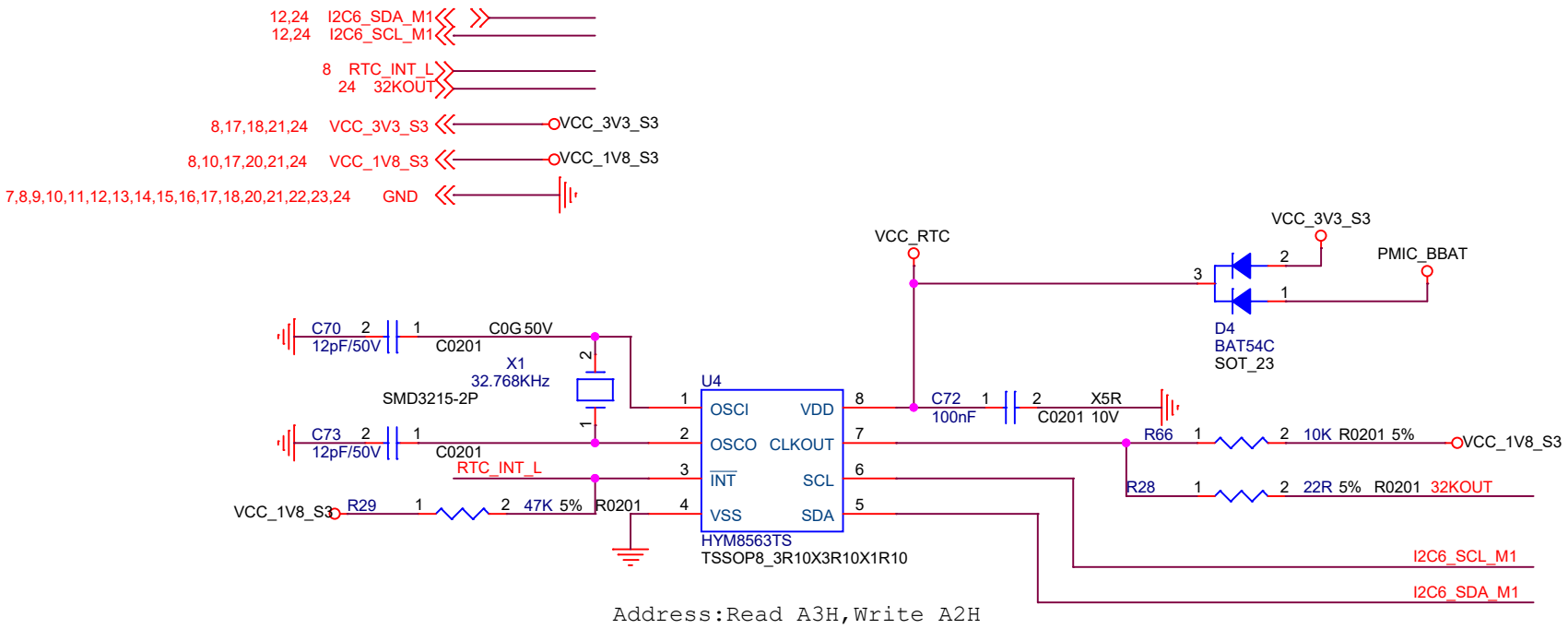


VCC4V0_SYS



armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	18.Power_Ext Discrete				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	18 of 24

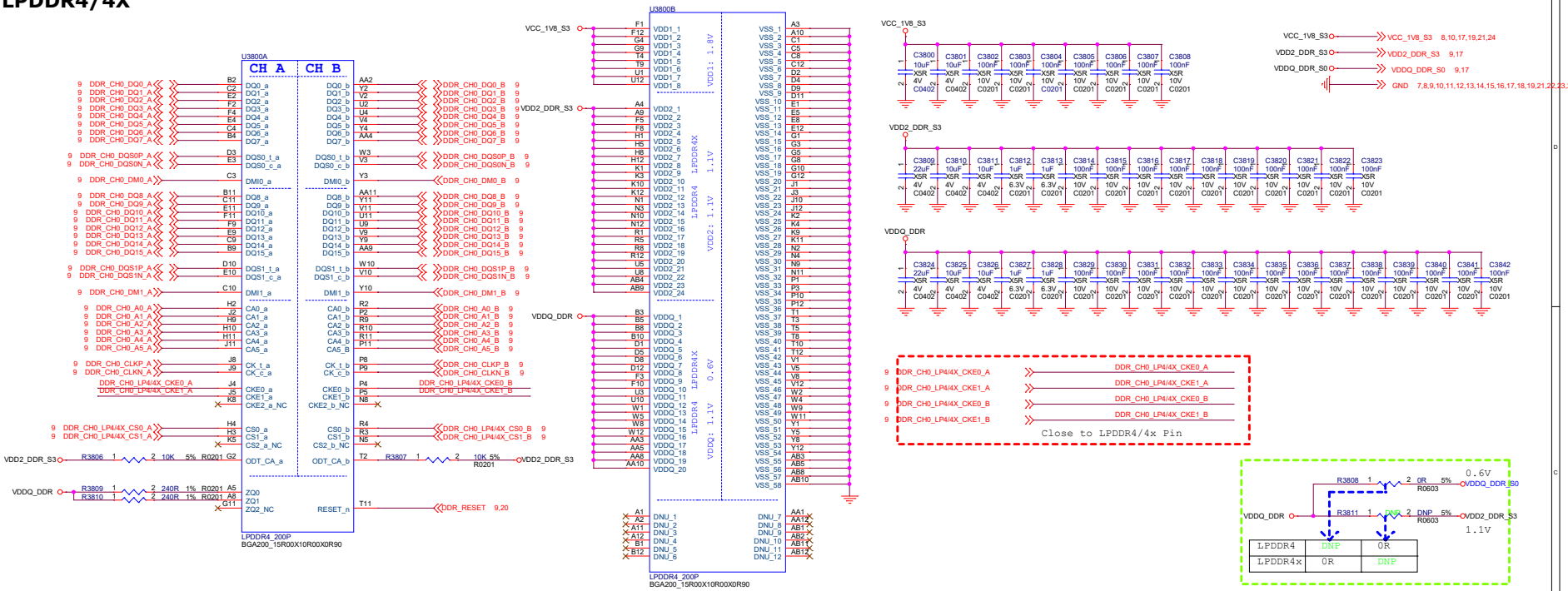
RTC IC

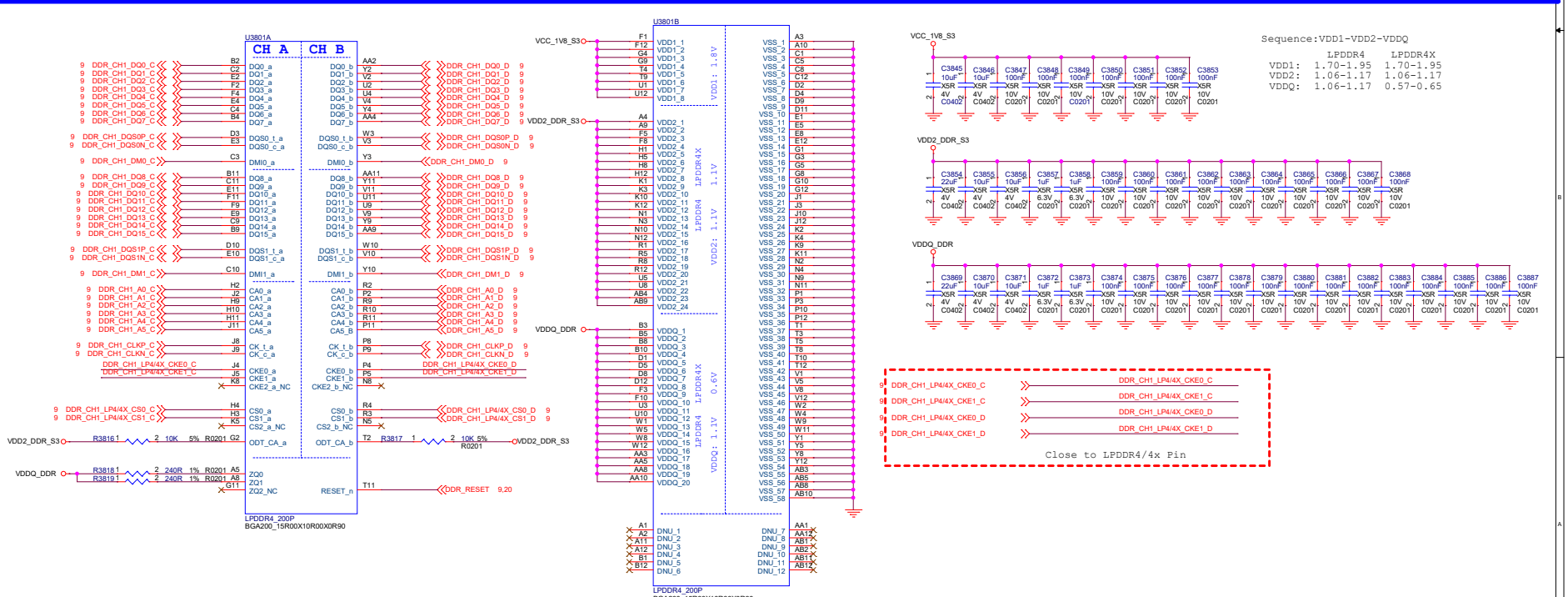


Address:Read A3H,Write A2H

armsom	ArmSoM				
Project:	ArmSoM-AIM7				
File:	19.RTC/FAN/POWER				
Date:	Wednesday, December 20, 2023			Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by:	<Checker>	Sheet:	19 of 24

LPDDR4/4X

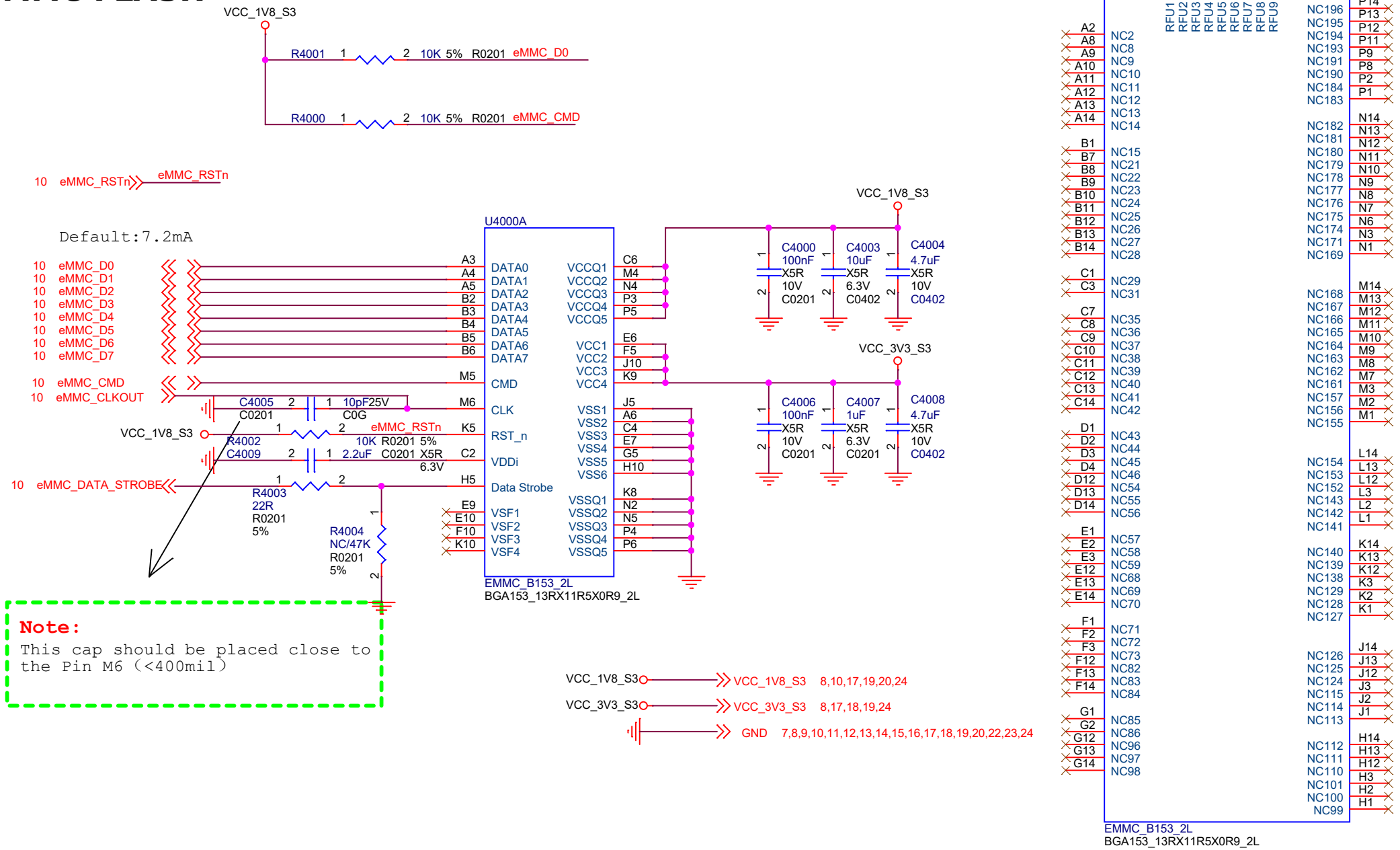




armsom	ArmSoM	
Project:	ArmSoM-AIM7	
File:	20.DRAM-LPDDR4X_200P_2X32bit	
Date:	Wednesday, December 20, 2023	Rev. V1.0
Designed by:	Liu Xinglin / Reviewed by: <Checker>	Sheet: 20 of 24

Rockchip Confidential

eMMC FLASH



armsom	ArmSoM		
Project:	ArmSoM-AIM7		
File:	21.Flash-eMMC Flash		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 21 of 24

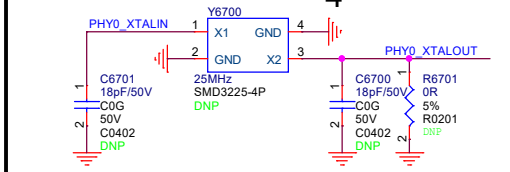
RGMII TO RJ45

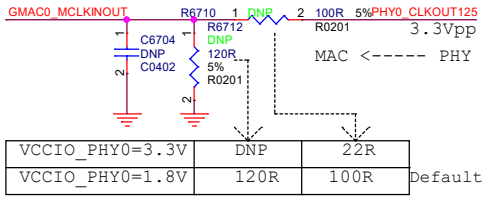
GMAC0_TXD0 12
GMAC0_TXD1 12
GMAC0_TXD2 12
GMAC0_TXD3 12
GMAC0_TXEN 12
GMAC0_TXCLK 12

GMAC0_RXD0 12
GMAC0_RXD1 12
GMAC0_RXD2 12
GMAC0_RXD3 12
GMAC0_RXDV_CRS 12

GMAC0_RXCLK 12
ETH0_REFCLKO_25M 12
GMAC0_MCLKINOUT 12
GMAC0_MDC 12
GMAC0_MDIO 12

GMAC0_RSTn_L 12

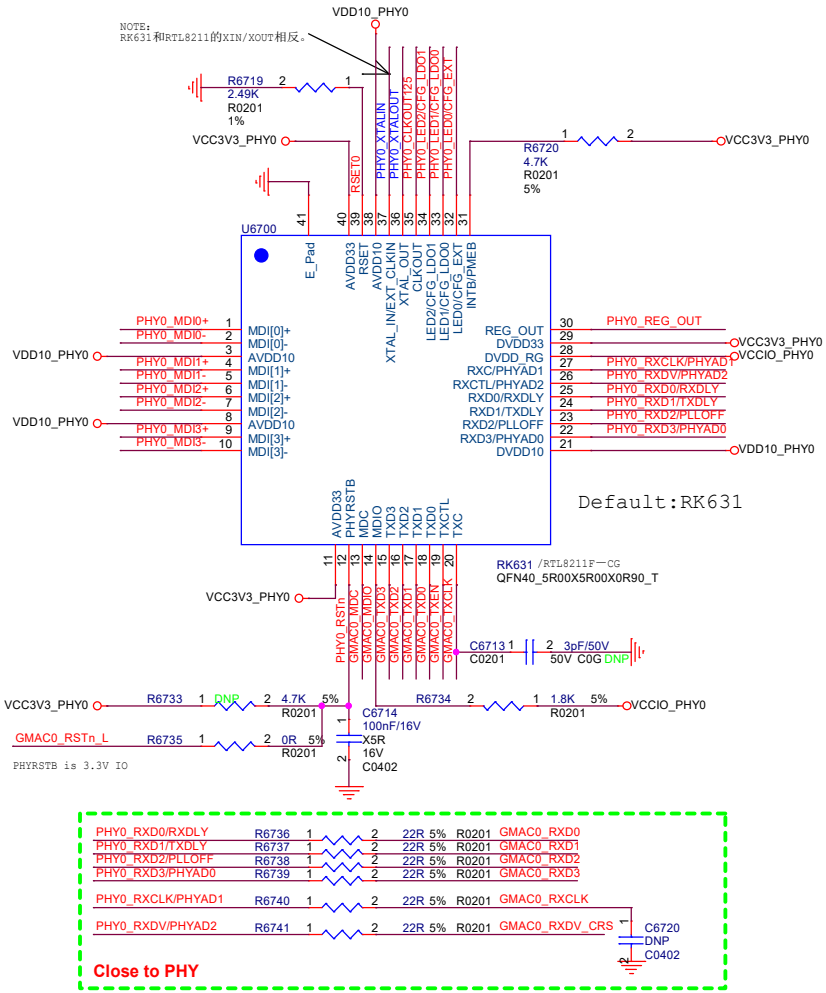


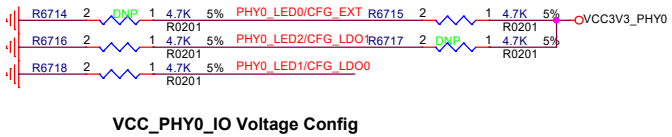


VCCIO_PHY0=3.3V	DNP	22R	Default
VCCIO_PHY0=1.8V	120R	100R	

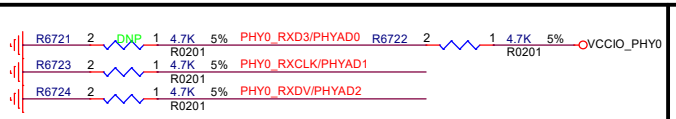
PHY0_MDI0- 24
PHY0_MDI0+ 24
PHY0_LED1/CFG_LDO0 24
PHY0_MDI1- 24
PHY0_MDI1+ 24
PHY0_LED2/CFG_LDO1 24
PHY0_MDI2- 24
PHY0_MDI2+ 24
PHY0_MDI3- 24
PHY0_MDI3+ 24

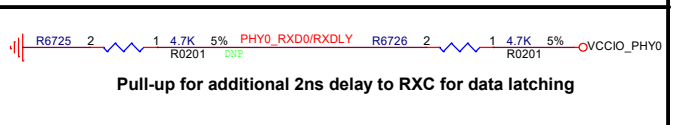
GND 7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,23

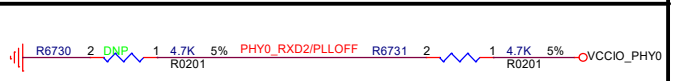


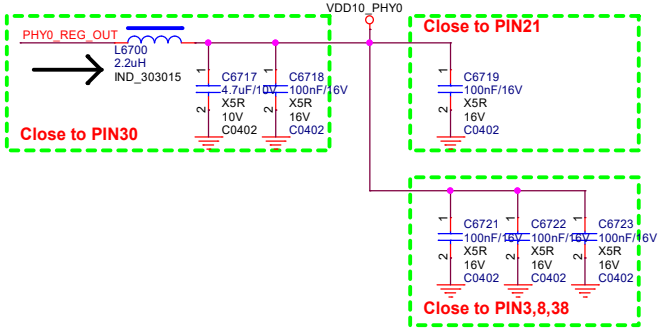


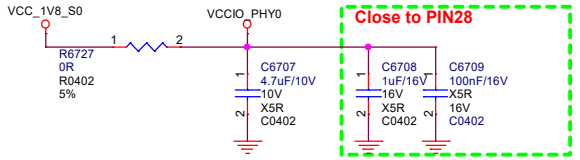
RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	
External 3.3V(default)	1'b1	2'b00	CFG_EXT: 1:External Power Source for IO pad. 0:Integrated LDO for IO pad CFG_LDO(1:0) 10:1.8V 00:3.3V
External 1.8V	1'b1	2'b10	
Internal 1.8V	1'b0	2'b10	

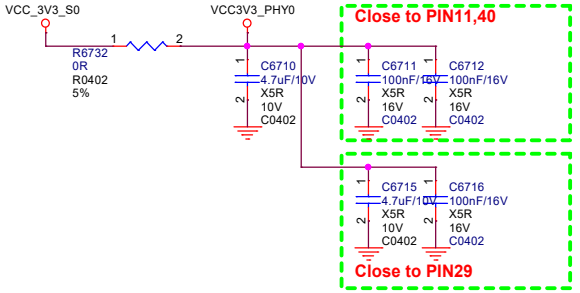








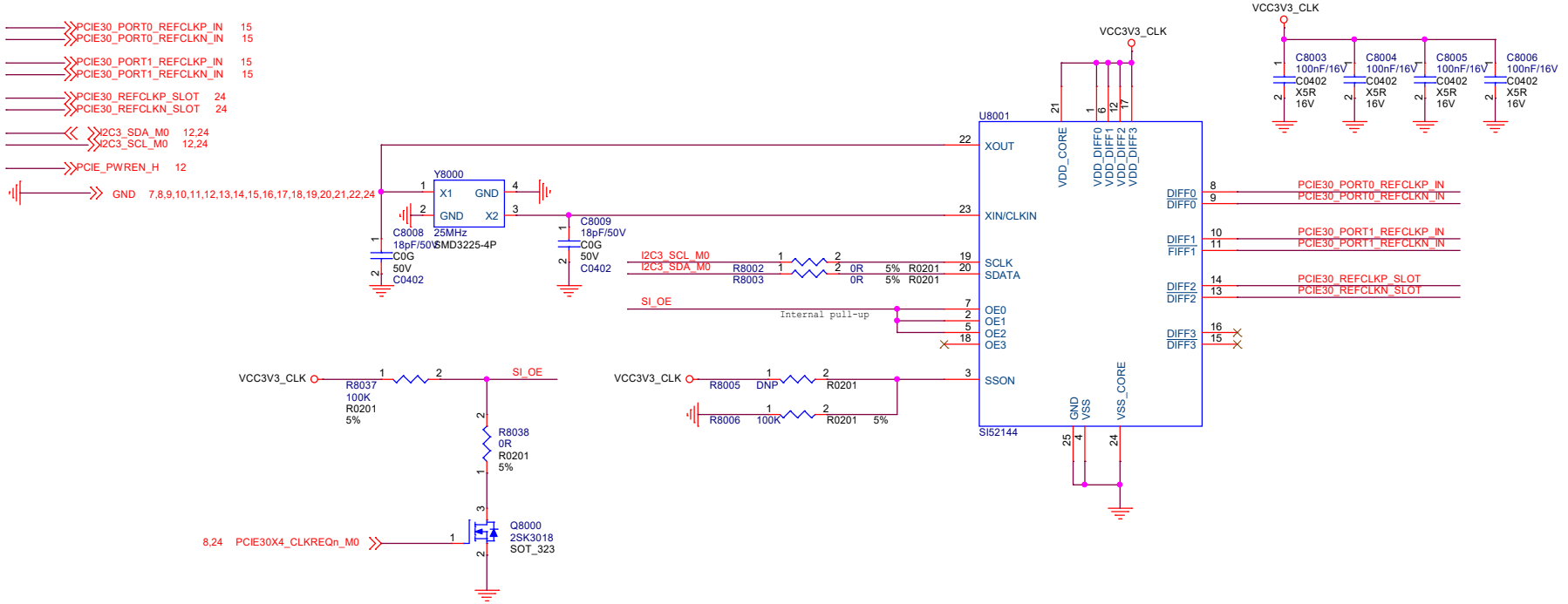




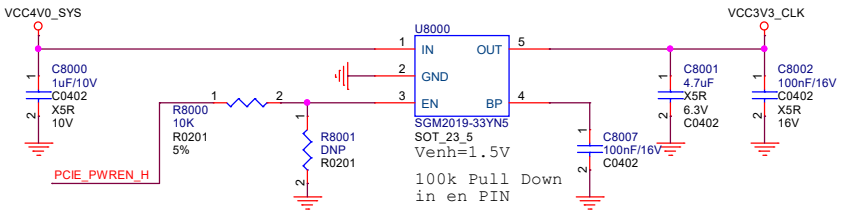
armsom ArmSoM

Project:	ArmSoM-AIM7		
File:	22.Ethernet-GPHY_RGMII1		
Date:	Wednesday, December 20, 2023	Rev:	V1.0
Designed by:	Liu Xinglin	Reviewed by: <Checker>	Sheet: 22 of 24

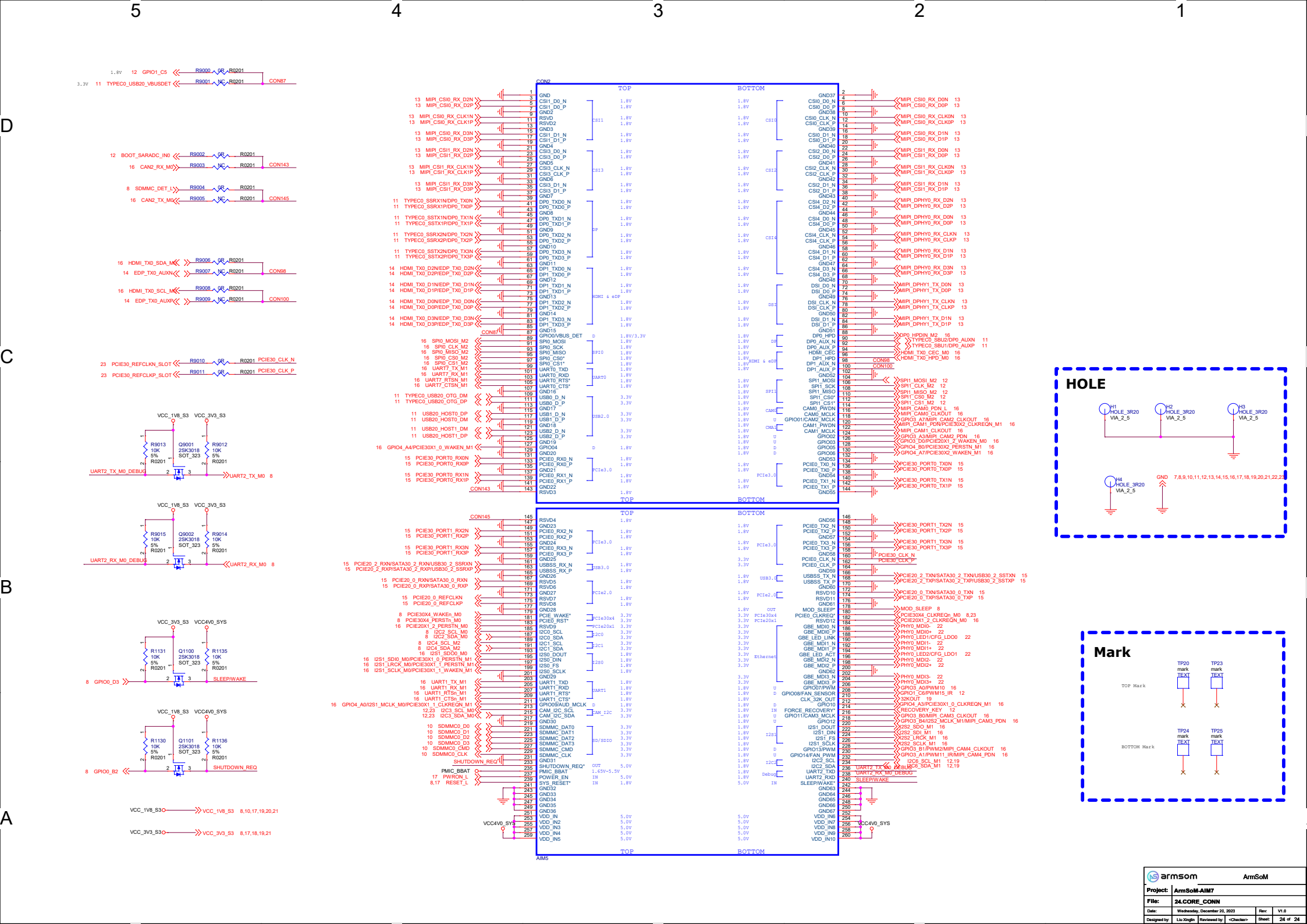
Crystal Generator



PCIe3.0 POWER



armsom	ArmSoM
Project:	ArmSoM-AIM7
File:	23.PCIE-PCIE3.0 CLK GENERATOR
Date:	Wednesday, December 20, 2023
Rev:	V1.0
Designed by:	Liu Xinglin
Reviewed by:	<Checker>
Sheet:	23 of 24


5
4
3
2
1
D
C
B
A
CON2
TOP
BOTTOM
HOLE
H1 HOLE_3R20 VIA_2_5
H2 HOLE_3R20 VIA_2_5
H3 HOLE_3R20 VIA_2_5
H4 HOLE_3R20 VIA_2_5
GND 7,8,9,10,11,12,13,14,15,16,17,18,19,20,21,22,23
Mark
TOP Mark
BOTTOM Mark
TP20 mark TEXT
TP23 mark TEXT
TP24 mark TEXT
TP25 mark TEXT
AIM5
armsom
ArmSoM
Project: ArmSoM-AIM7
File: 24.CORE_CONN
Date: Wednesday, December 20, 2023
Rev: V1.0
Designed by: Liu Xinglin
Reviewed by: <Checker>
Sheet: 24 of 24