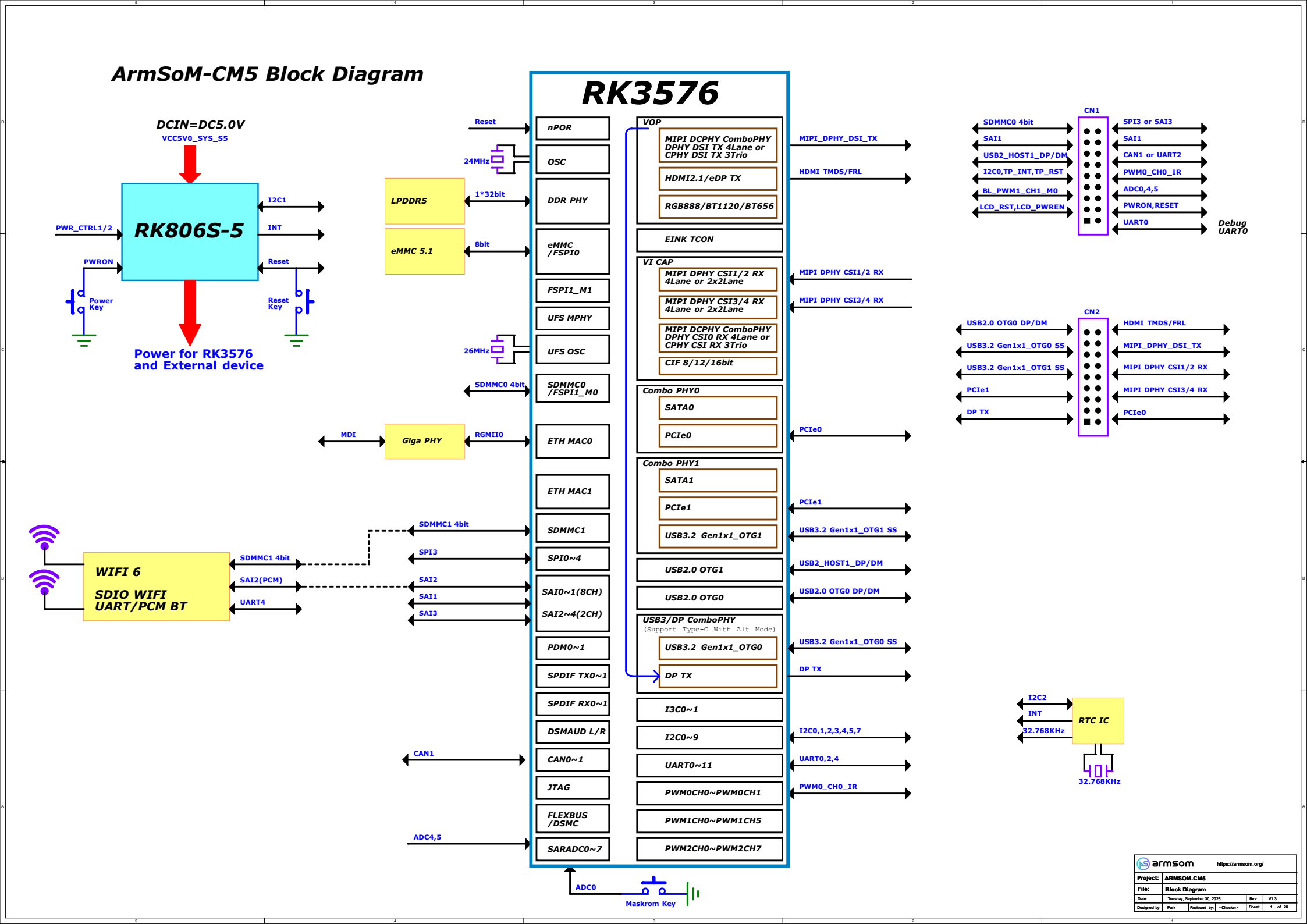
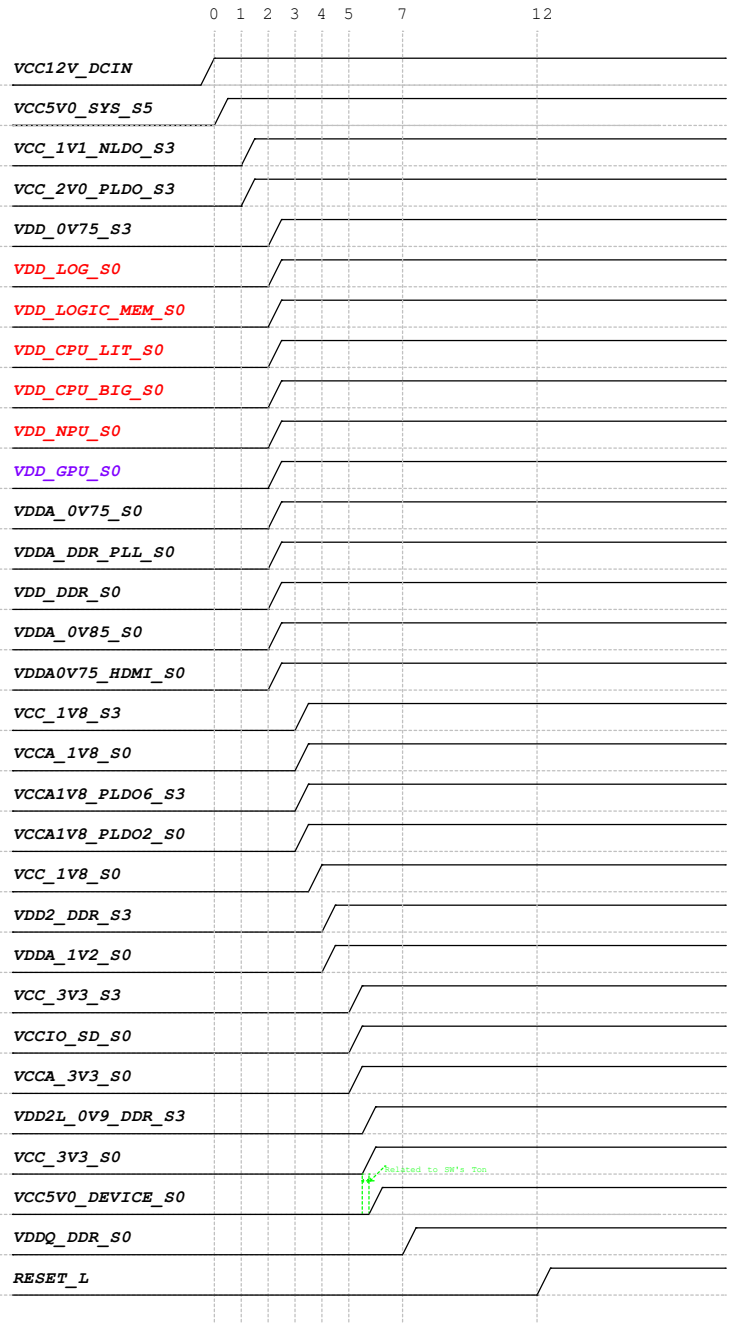
ArmSoM-CM5 Block Diagram



armsom	https://armsom.org/
Project:	ARMSOM-CM5
File:	Block Diagram
Date:	Tuesday, September 30, 2025
Rev:	V1.3
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	1 of 20

Power Sequence



Power description

Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Work Voltage	Peak Current	Sleep Current
VCC5V0_SYS_S5	RK806_BUCK1	6.5A	VDD_CPU_BIG_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK2	5A	VDD_NPU_S0	Slot:2	0.75V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK3	5A	VDD_CPU_LIT_S0	Slot:2	0.85V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK4	5A	VCC_3V3_S3	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK5	3A	VDD_GPU_S0	Slot:2	ADJ FB=0.5V	ON	DVFS	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK6	3A	VDDQ_DDR_S0	Slot:7	ADJ FB=0.5V	ON	0.61V-LP4/4x 0.51V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK7	3A	VDD_LOGIC_S0 VDD_LOGIC_MEM_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK8	3A	VCC_1V8_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK9	3A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	1.1V-LP4/4x 1.05V-LP5	TBD	TBD
VCC5V0_SYS_S5	RK806_BUCK10	3A	VDD_DDR_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
VCC_2V0_PLDO	RK806_PLDO1	0.5A	VCCA_1V8_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO2	0.3A	VCCA1V8_PLDO2_S0	Slot:3	1.8V	ON	1.8V	TBD	TBD
	RK806_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	1.2V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO4	0.5A	VCCA_3V3_S0	Slot:5	3.0V	ON	3.3V	TBD	TBD
	RK806_PLDO5	0.3A	VCCIO_SD_S0	Slot:5	3.3V	ON	3.3V	TBD	TBD
VCC5V0_SYS_S5	RK806_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	1.8V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	0.85V DVFS	TBD	TBD
	RK806_NLDO3	0.5A	VDDA0V75_HDMI_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
VCC_1V1_NLDO	RK806_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	0.85V	TBD	TBD
	RK806_NLDO5	0.3A	VDDA_0V75_S0	Slot:2	0.75V	ON	0.75V	TBD	TBD
	RK806_RESETn								
VCC5V0_SYS_S5	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5A	0.9V	ON	0.9V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_2V0_PLDO_S3	Slot:1	2.1V	ON	2.0V	TBD	TBD
VCC5V0_SYS_S5	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	1.1V	TBD	TBD
VCC12V_DCIN	EXT BUCK	5A	VCC5V0_SYS_S5	Slot:0	5.0V	ON	5.0V	TBD	TBD
VCC12V_DCIN	EXT BUCK	3A	VCC5V0_DEVICE_S0	Slot:5A	5.2V	ON	5.2V	TBD	TBD
VCC_3V3_S3	SWITCH	2A	VCC_3V3_S0	Slot:5A	3.3V	ON	3.3V	TBD	TBD
VCC_1V8_S3	SWITCH	2A	VCC_1V8_S0	Slot:3A	1.8V	ON	1.8V	TBD	TBD

Note:

The power suffix S0, S3 or S5 means:
S5: Keep power on during power down
S3: Keep power on during sleeping
S0: Power off during sleeping

Note:

Peripherals connected to the GPIO of SOC need to consider the leakage between the GPIO of SOC and the Peripherals. It is recommended to power on both the Peripherals's power supply and the SOC's GPIO power supply simultaneously.

IO Power Domain Map

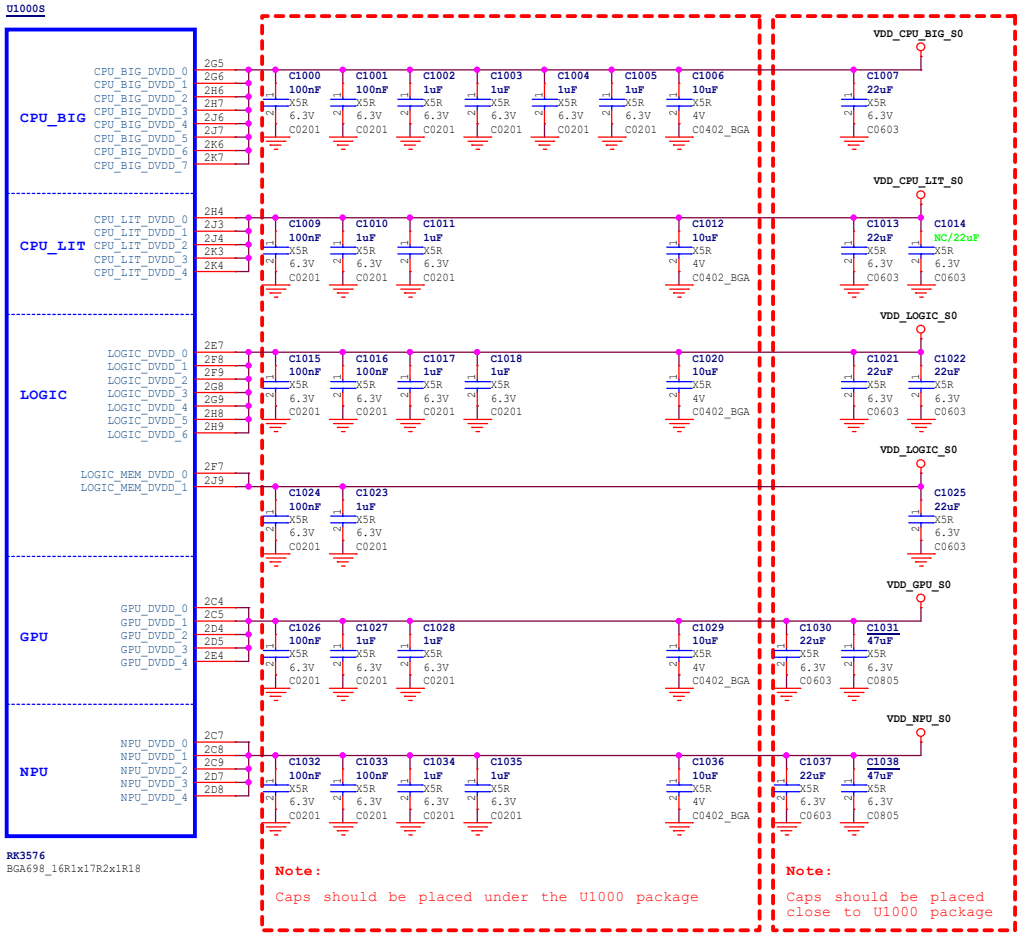
IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO0	Pin 2K11	1.8V Only	PMUIO0_VCC1V8	VCC_1V8	1.8V
PMUIO1	Pin 1U20	1.8V or 3.3V	PMUIO1_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO0	Pin 1J20	1.8V Only	VCCIO0_VCC1V8	VCC_1V8	1.8V
VCCIO1	Pin 2A8	1.8V or 3.3V	VCCIO1_VCC	VCC_1V8 VCC_3V3	1.8V/3.3V
VCCIO2	Pin 2A2	1.8V or 3.3V	VCCIO2_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO3	Pin 2B10	1.8V or 3.3V	VCCIO3_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO4	Pin 2A7	1.8V or 3.3V	VCCIO4_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO5	Pin 2A4/2A5	1.8V or 3.3V	VCCIO5_VCC	VCC_1V8 VCC_3V3	1.8V
VCCIO6	Pin 2N3	1.8V or 3.3V	VCCIO6_VCC	VCC_1V8 VCC_3V3	3.3V
VCCIO7	Pin 2M3	1.2V or 1.8V	VCCIO7_VCC	VCC_1V2 VCC_1V8	1.2V

IO Type	Operating Voltage
1.8V Only	VCCIO*_VCC1V8=1.8V
1.2V or 1.8V	VCCIO*_VCC=1.2V or 1.8V
1.8V or 3.3V	VCCIO*_VCC=1.8V or 3.3V

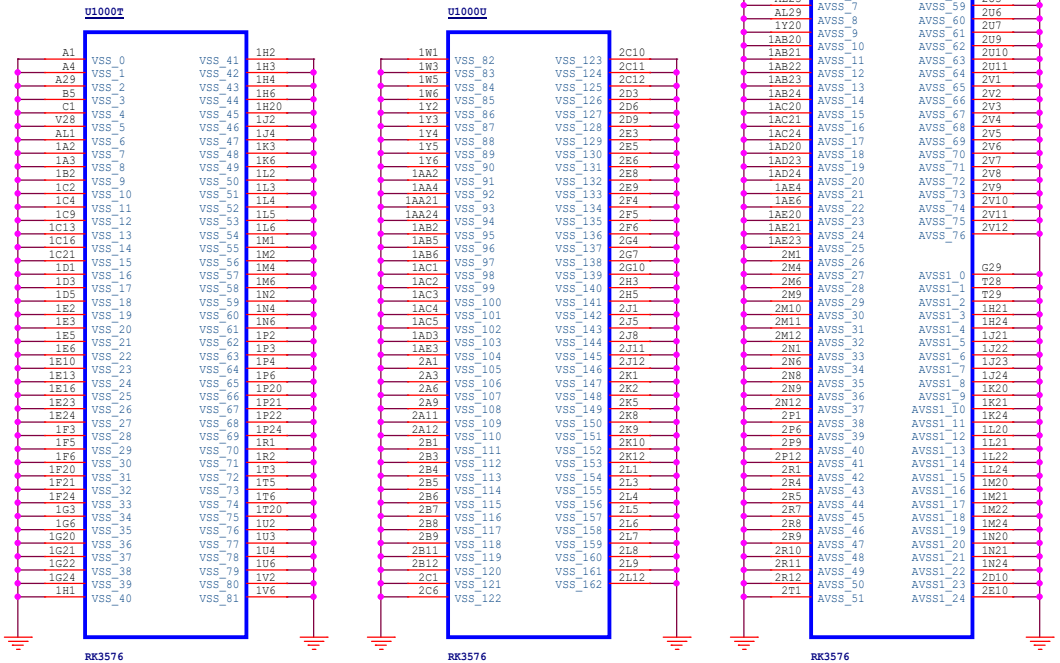
armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	Power Sequence and Map				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 20

RK3576_S (Power)



RK3576_T/U/V (GND)



armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	RK3576-Power/GND		
Date:	Tuesday, September 30, 2025	Rev:	V1.3
Designed by: Park	Reviewed by: <Checker>	Sheet:	3 of 20

RK3576_E (PMUIO0/1)

U1000E

OSC

PMUIO0 Domain
Operating Voltage=1.8V

PLL

PMUIO1 Domain
Operating Voltage=1.8V/3.3V

PMUIO0/PMUIO1/VCCIO7 Domain Logic Power
Operating Voltage=0.75V

RK3576
BGA698_16R1x17R2x1R18

RK3576_R (SARADC)

U1000R

SARADC
12-bit 1MS/s

TSADC

OTP

RK3576
BGA698_16R1x17R2x1R18

BOOT MODE CONFIG

Config Table for SARADC_VIN0_BOOT

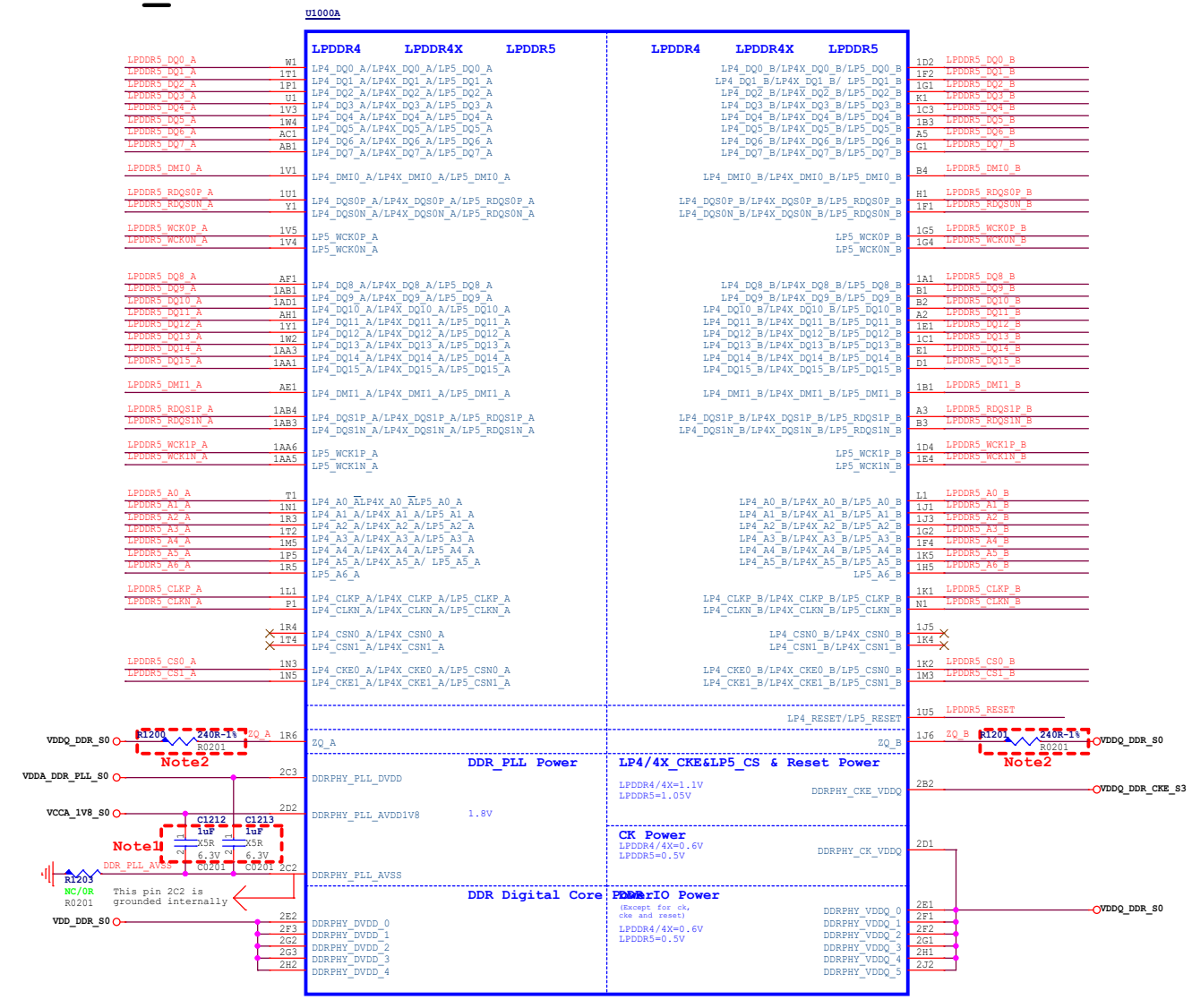
Item	Rup	Rdown	ADC Value	Boot Mode
Config1	NC	10K	0	USB (Maskrom mode)
Config2	100K	11.3K	416	FSPI0->USB
Config3	100K	24.9K	816	FSPI1_M0->EMMC->USB
Config4	100K	43K	1231	FSPI1_M1->EMMC->USB
Config5	100K	68K	1658	FSPI0->UFS->USB
Config6	100K	100K	2048	FSPI1_M0->UFS->USB
Config7	68K	100K	2438	UFS->USB
Config8	43K	100K	2864	UFS->SDMMC0->USB
Config9	24.9K	100K	3279	RFU
Config10	11.3K	100K	3679	EMMC->SDMMC0->USB
Config11	10K	NC	4095	EMMC->USB

Note:
Must be mounted

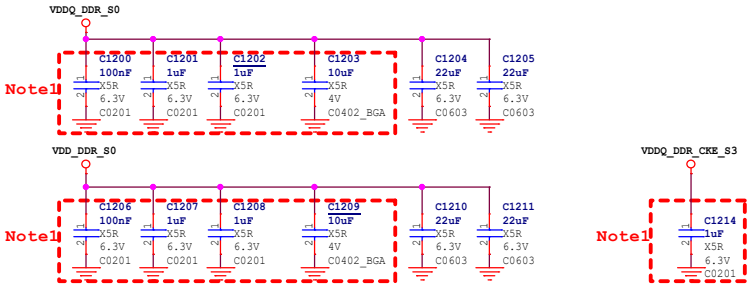
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	RK3576-OSC/PLL/PMUIO/SARADC		
Date:	Tuesday, September 30, 2025	Rev:	V1.3
Designed by: Park	Reviewed by: <Checker>	Sheet:	4 of 20

RK3576_A(DDRPHY)



DDR FILTER

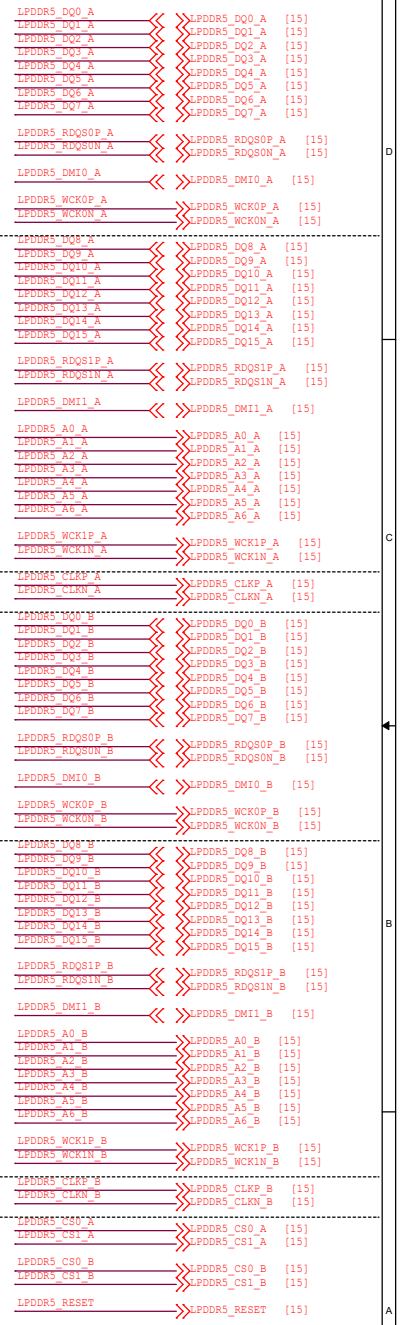


Note:
(1) Power Sequence: VDD-VDDQ_CKE-VDDQ
(2) Hold power of DDRPHY_CKE_VDDQ during retention times.

Note1:
Caps in the red line dotted box should be placed under the U1000 package

Note2:
Resistors in the red line dotted box should be placed under the U1000 package

LPDDR5



armsom https://armsom.org/

Project:	ARMSOM-CM5		
File:	RK3576-DDR PHY		
Date:	Tuesday, September 30, 2025	Rev:	V1.4
Designed by:	Park	Reviewed by: <Checker>	Sheet: 5 of 20

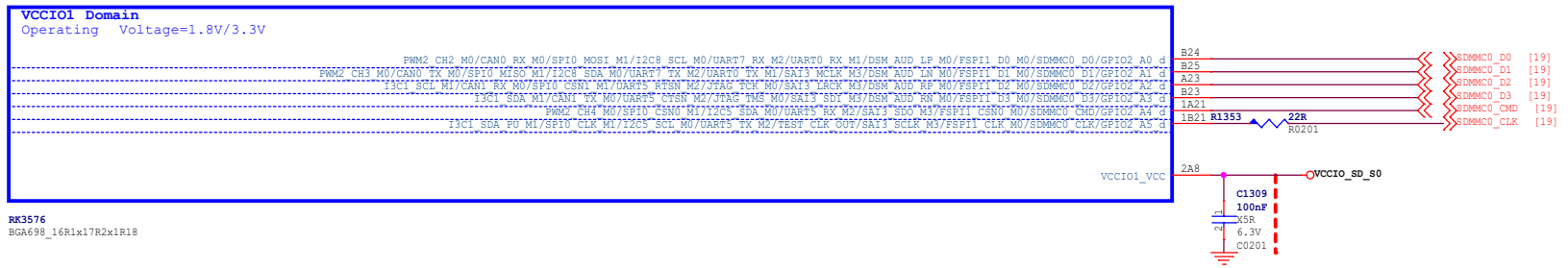
RK3576_B (UFS2.1)



RK3576_C (VCCIO0)



RK3576_D (VCCIO1)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	RK3576-eMMC/UFS/SD				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 20

RK3576_L (USB3/DP)

USB3 OTG0/DP1.4 Alt
USB:USB3.2 Gen1x1 OTG0
DP :RBR/HBR/HBR2/HBR3

Support:Type-C With Displayport Alternate Mode

Diff 100 Ohm ± 10%

DP_TX_AUXP
DP_TX_AUXN

Diff 95 Ohm ± 10%

USB3_OTG0_SSRX1P/DP_TX_D0P
USB3_OTG0_SSRX1N/DP_TX_D0N
USB3_OTG0_SSTX1P/DP_TX_D1P
USB3_OTG0_SSTX1N/DP_TX_D1N
USB3_OTG0_SSRX2P/DP_TX_D2P
USB3_OTG0_SSRX2N/DP_TX_D2N
USB3_OTG0_SSTX2P/DP_TX_D3P
USB3_OTG0_SSTX2N/DP_TX_D3N
USB3_OTG0_REXT/DP_TX_REXT
USB3_OTG0_DP_TX_AVDD0V85
USB3_OTG0_DP_TX_DVDD0V85
USB3_OTG0_DP_TX_AVDD1V8

2T2 DP_TX_AUXP [19]
2T3 DP_TX_AUXN [19]
AK10 USB3_OTG0_SSRX1P/D0P [19]
AL10 USB3_OTG0_SSRX1N/D0N [19]
AL11 USB3_OTG0_SSTX1P/D1P [19]
AK11 USB3_OTG0_SSTX1N/D1N [19]
AK12 USB3_OTG0_SSRX2P/D2P [19]
AL12 USB3_OTG0_SSRX2N/D2N [19]
AL13 USB3_OTG0_SSTX2P/D3P [19]
AK13 USB3_OTG0_SSTX2N/D3N [19]
2T7 USB3_OTG0_DP_TX_REXT R1400 8.2K-1% R0201
2M5 VDDA_0V85_S0
2N5 C1400 1uF X5R 6.3V C0201
2N4 VCCA_1V8_S0
C1402 1uF X5R 6.3V C0201

U1000L
RK3576
BGA698_16R1x17R2x1R18

MODE1: TypeC with ALT (Default)

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_M (USB2)

USB2 OTG0
OTG/HOST/DEVICE
HS/FS/LS
Download Port

USB2 OTG1
OTG/HOST/DEVICE
HS/FS/LS

Diff 90 Ohm ± 10%

USB2_OTG0_DP
USB2_OTG0_DM
USB2_OTG0_ID
USB2_OTG0_VBUSDET
USB2_OTG0_REXT
USB2_OTG1_DP
USB2_OTG1_DM
USB2_OTG1_ID
USB2_OTG1_VBUSDET
USB2_OTG1_REXT
USB2_OTG_DVDD0V75
USB2_OTG_AVDD1V8
USB2_OTG_AVDD3V3

40K

AK9 USB2_OTG0_DP [19]
AL9 USB2_OTG0_DM [19]
2R6 Note: There is an internal pull-up resistor connected to 1.8V
USB2_OTG0_ID [19]
2P3 USB2_OTG0_VBUSDET
2R3 USB2_OTG0_REXT R1401 200R-1% R0201
C1404 100nF X5R 10V C0201
R7016 4.7K R0201 VCC_3V3_S0
2T4 USB2_HOST1_DP [19]
2T5 USB2_HOST1_DM [19]
2T9
2T10 R1407 NC/4.7K R0201 VCC_3V3_S0
2U8 USB2_OTG1_REXT R1402 200R-1% R0201
2P5 VDDA_0V75_S0
C1405 100nF X5R 6.3V C0201
2P4 VCCA_1V8_S0
C1406 100nF X5R 6.3V C0201
2P7 VCC_3V3_S0
C1408 100nF X5R 6.3V C0201

Note!!!
The USB2 OTG1 function cannot be used, if the PCIe1 or SATA1 function of Combo PHY1 is selected

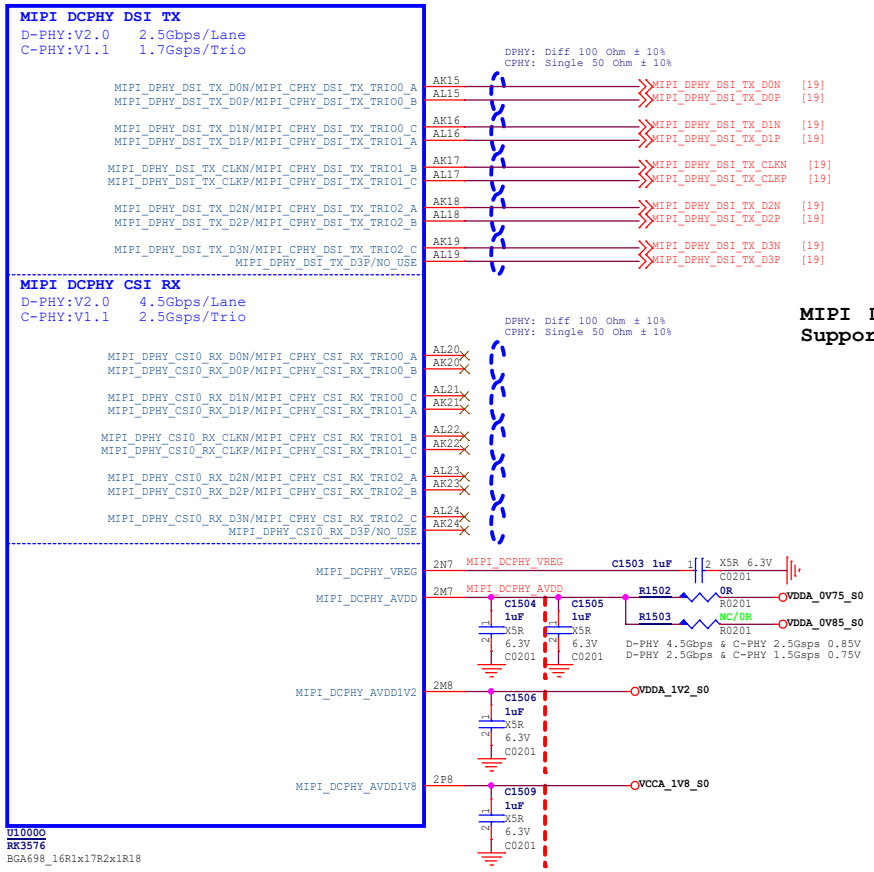
U1000M
RK3576
BGA698_16R1x17R2x1R18

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	RK3576-TypeC/USB				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 20

RK3576_O(MIPI DCPHY)

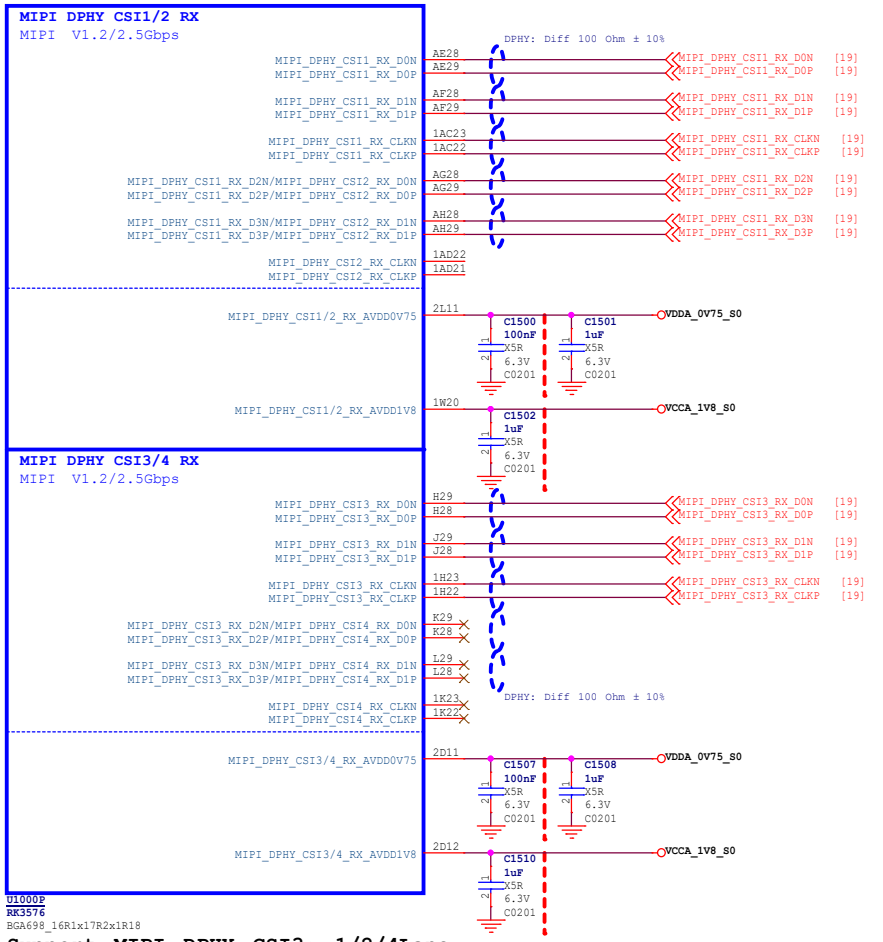


MIPI DPHY CSI0:
Support 1/2/4Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

RK3576_P(MIPI DPHY CSI RX)

Support MIPI DPHY CSI1: 1/2/4Lane
Support MIPI DPHY CSI2: 1/2Lane
Support: MIPI DPHY CSI1 2Lane + MIPI DPHY CSI2 2Lane



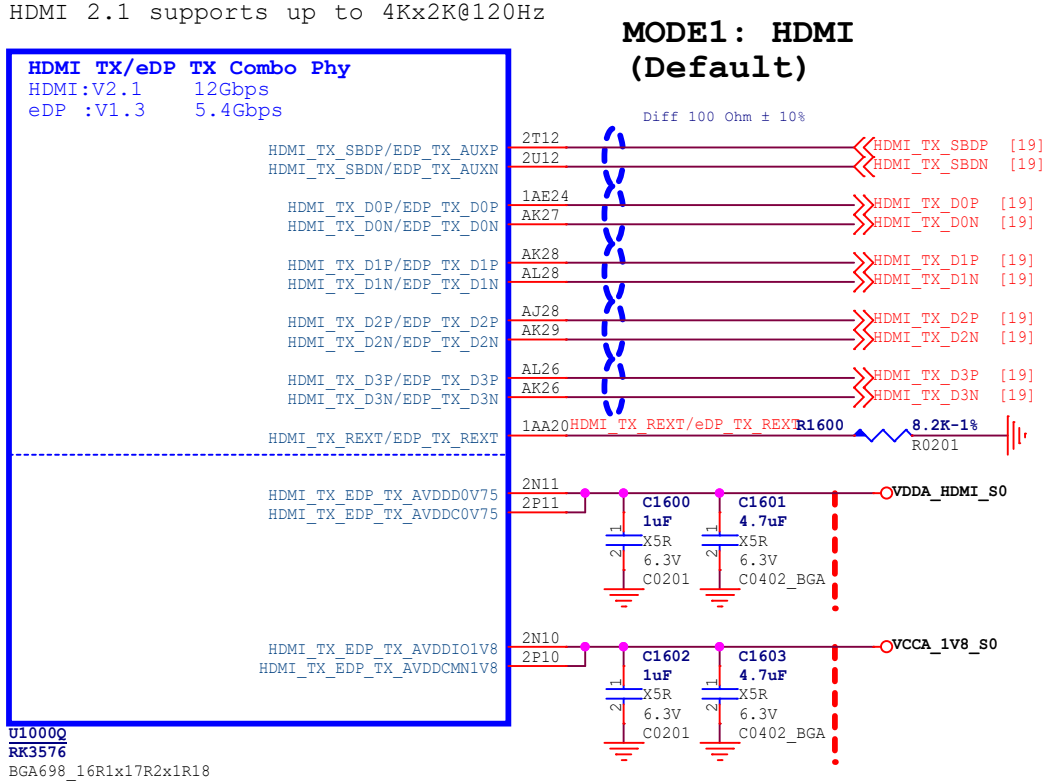
Support MIPI DPHY CSI3: 1/2/4Lane
Support MIPI DPHY CSI4: 1/2Lane
Support MIPI DPHY CSI3 2Lane + MIPI DPHY CSI4 2Lane

Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	RK3576-MIPI DSI/CSI				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 20

RK3576_Q(HDMI/eDP)

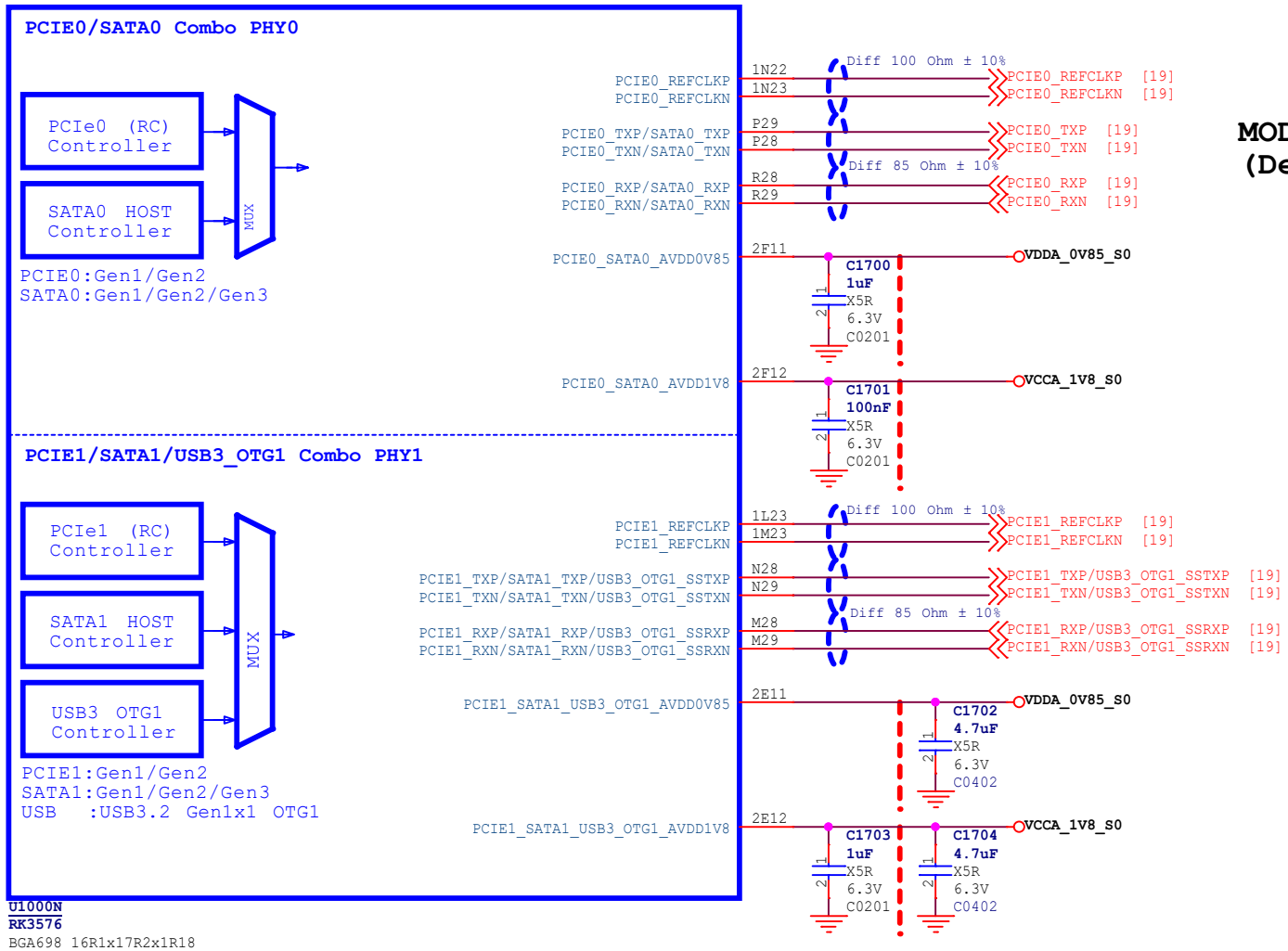
Note:
HDMI 2.1 supports up to 4Kx2K@120Hz



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	RK3576-HDMI/eDP				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 20

RK3576_N(PCIe/SATA/USB3)



MODE1: PCIe0 (Default)

Note!!!

If the PCIe1 or SATA1 function of Combo PHY1 is selected, the USB3 OTG1 function cannot be used, and even the USB2 OTG1 function cannot be used

Note:

Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

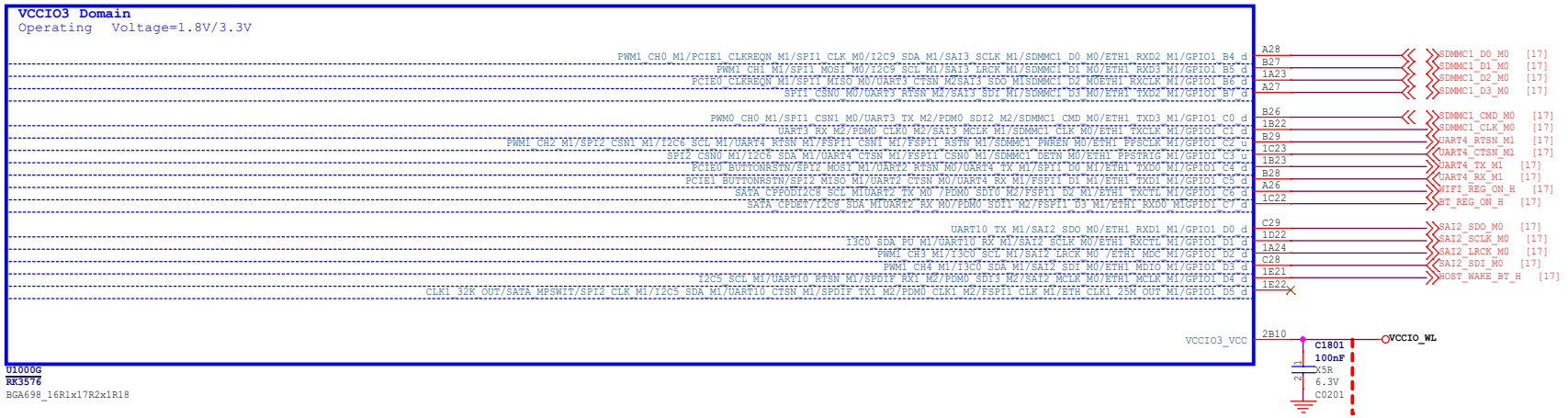
armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	RK3576-PCIe/SATA/USB3				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	10 of 20

RK3576_F(VCCIO2)



MODE1: HDMI RX Audio (Default)

RK3576_G(VCCIO3)



RK3576_J(VCCIO6)



Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	RK3576-GPIO VCCIO2/3/6				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	11 of 20

RK3576_H(VCCIO4)

VCCIO4 Domain
Operating Voltage=1.8V/3.3V

I2C4_SCL_M2/SPI4_CSN1_M3/UART8_TX_M1/SAI0_SDO0_M0/ETH0_RXD0_M1/SDMMC1_D0_M1/VI_CIF_D15/GPIO2_A6_d
I2C4_SDA_M2/UART8_RX_M1/SAI0_SDO1_M0/ETH0_TXCTL_M1/SDMMC1_D1_M1/VI_CIF_D14/GPIO2_A7_d
UART1_TX_M1/PDM0_SDI3_M3/SAI0_SDI0_M0/ETH0_TXD1_M1/SDMMC1_D2_M1/VI_CIF_D13/GPIO2_B0_d
UART1_RX_M1/PDM0_SDI2_M3/SAI0_SDI1_M0/ETH0_RXD0_M1/SDMMC1_D3_M1/VI_CIF_D12/GPIO2_B1_d
PCIE0_CLKREQN_M0/SPI4_CSN0_M3/UART1_CTSN_M1/PDM0_SDI1_M3/SAI0_SDI2_M0/ETH0_TXD3_M1/SDMMC1_CMD_M1/VI_CIF_D11/GPIO2_B2_d
PCIE1_CLKREQN_M0/SPI4_CLK_M3/UART1_RTSN_M1/PDM0_CLK1_M3/SAI0_SDO2_M0/ETH0_TXCLK_M1/SDMMC1_CLK_M1/VI_CIF_D10/GPIO2_B3_d
SATA0_ACTLED_M0/SPI4_MOSI_M3/UART7_CTSN_M0/PDM0_SDI0_M3/SAI0_SDI3_M0/ETH0_TXD2_M1/SDMMC1_PWREN_M1/VI_CIF_D9/GPIO2_B4_d
SATA1_ACTLED_M0/SPI4_MISO_M3/UART7_RTSN_M0/PDM0_CLK0_M3/SAI0_MCLK_M0/ETH0_RXCLK_M1/SDMMC1_DETN_M1/VI_CIF_D8/GPIO2_B5_d
I2C8_SCL_M2/UART8_RTSN_M1/UART7_TX_M0/SAI0_SCLK_M0/ETH0_RXD3_M1/ETH1_PTP_REFCLK_M1/VI_CIF_D7/GPIO2_B6_d
I2C8_SDA_M2/UART8_CTSN_M1/UART7_RX_M0/SAI0_LRCK_M0/ETH0_RXD2_M1/VI_CIF_D6/GPIO2_B7_d
PWM1_CH0_M2/UART9_RX_M0/PDM1_SDI1_M0/ETH0_PTP_REFCLK_M1/ETH1_RXD2_M0/VI_CIF_D5/GPIO2_C0_d
PWM1_CH1_M2/SPI1_CSN1_M1/UART9_TX_M0/PDM1_CLK1_M0/SAI2_MCLK_M1/ETH0_PPSCLK_M1/ETH1_RXD3_M0/VI_CIF_D4/GPIO2_C1_d
PWM1_CH2_M2/SPI1_MOSI_M1/UART11_CTSN_M1/PDM1_SDI2_M0/SAI2_SCLK_M1/ETH0_PPSTRIG_M1/ETH1_RXCLK_M0/VI_CIF_D3/GPIO2_C2_d
PWM0_CH0_M2/SPI1_MISO_M1/UART11_RTSN_M1/PDM1_SDI3_M0/SAI2_LRCK_M1/ETH1_TXD2_M0/VI_CIF_D2/GPIO2_C3_d
PWM1_CH3_M2/SPI1_CSN0_M1/UART11_TX_M1/PDM1_SDI0_M0/SAI2_SDO_M1/ETH1_TXD3_M0/VI_CIF_D1/GPIO2_C4_d
PWM1_CH4_M2/SPI1_CLK_M1/UART11_RX_M1/PDM1_CLK0_M0/SAI2_SDI_M1/ETH1_TXCLK_M0/VI_CIF_D0/GPIO2_C5_d
PWM1_CH5_M2/I2C5_SCL_M2/UART4_CTSN_M0/SAI4_SCLK_M3/ETH1_TXD0_M0/GPIO2_C6_d
PWM0_CH7_M2/I2C5_SDA_M2/UART4_RTSN_M0/SAI4_LRCK_M3/ETH1_TXD1_M0/GPIO2_C7_d
PWM2_CH0_M2/I2C6_SCL_M2/UART4_TX_M0/SAI4_SDI_M3/ETH1_TXCTL_M0/GPIO2_D0_d
PWM2_CH1_M2/I2C6_SDA_M2/UART4_RX_M0/SAI4_SDO_M3/ETH1_RXD0_M0/GPIO2_D1_d
PWM2_CH2_M2/I3C1_SCL_M0/UART6_TX_M1/SAI4_MCLK_M3/ETH1_RXD1_M0/CAM_CLK0_OUT_M1/GPIO2_D2_d
PWM2_CH3_M2/I3C1_SDA_M0/UART6_RX_M1/ETH1_RXCTL_M0/GPIO2_D3_d
PWM2_CH4_M2/I2C9_SDA_M2/UART6_RTSN_M1/ETH1_MDC_M0/FSP_PRELIGHT_TRIG_M0/GPIO2_D4_d
PWM2_CH5_M2/I2C9_SCL_M2/UART6_CTSN_M1/ETH1_MDIO_M0/FSP_FLASH_TRIGOUT_M0/GPIO2_D5_d
PWM2_CH6_M2/I3C1_SDA_F0_M0/UART9_RTSN_M0/SPDIF_RX0_M2/SAI3_MCLK_M2/ETH0_MCLK_M1/ETH_CLK1_25M_OUT_M0/CAM_CLK1_OUT_M1/GPIO2_D6_d
PWM2_CH7_M2/SPI3_CSN1_M0/UART9_CTSN_M0/SPDIF_TX0_M2/SAI0_SDO3_M0/ETH_CLK0_25M_OUT_M1/ETH1_MCLK_M0/CAM_CLK2_OUT_M1/GPIO2_D7_d
I2C7_SCL_M1/SPI3_CLK_M0/UART3_TX_M0/SAI3_SCLK_M2/ETH0_MDIO_M1/VI_CIF_HREF/GPIO3_A0_d
I2C7_SDA_M1/SPI3_MOSI_M0/UART3_RX_M0/SAI3_LRCK_M2/ETH0_MDC_M1/ETH1_PPSTRIG_M0/VI_CIF_VSYNC/GPIO3_A1_d
MIPI_TE_M1/CAN1_TX_M3/SPI3_MISO_M0/UART3_CTSN_M0/SPDIF_RX1_M1/SAI3_SDO_M2/ETH0_RXCTL_M1/ETH1_PPSCLK_M0/VI_CIF_CLK0/GPIO3_A2_d
CAN1_RX_M3/SPI3_CSN0_M0/UART3_RTSN_M0/SPDIF_TX1_M1/SAI3_SDI_M2/ETH0_RXD1_M1/ETH1_PTP_REFCLK_M0/VI_CIF_CLK1/GPIO3_A3_d

B22
B20
B19
1A18
1A17
1B16
A19
1C18
A21
B21
A17
1A15
1D15
A15
1A13
1C15
1A14
B15
B16
1A16
B17
B18
1B13
1B15
1D18
1E15
1D16
1B18
1A20
1A19

PCIE0_PERSTn [19]
PCIE0_CLKREQn_M0 [19]
GMAC0_RSTn [18]
MIPI_DPHY_CSI_CAM1_RST_H [19]
OTG0_PWREN_H/UART7_TX/I2C8_SCL [19]
HP_DET_L/UART7_RX/I2C8_SDA [19]
LED_GREEN_EN/UART4_TX/I2C6_SCL [19]
LED_RED_EN/UART4_RX/I2C6_SDA [19]
PWM2_CH6_M2/SAI3_MCLK_M2 [19]
CAM_CLK2_OUT_M1_3V3 [19]
SPI3_CLK_M0/SAI3_SCLK_M2 [19]
SPI3_MOSI_M0/SAI3_LRCK_M2 [19]
SPI3_MISO_M0/SAI3_SDO_M2 [19]
SPI3_CSN0_M0/SAI3_SDI_M2 [19]

VCCIO4_VCC 2A7

C1900 NC/100nF X5R 6.3V C0201
C1901 1uF X5R 6.3V C0201
VCC_3V3_S0

U1000H
RK3576
BGA698_16R1x17R2x1R18

RK3576_I(VCCIO5)

VCCIO5 Domain
Operating Voltage=1.8V/3.3V

PWM1_CH0_M3/SPI2_CLK_M2/UART1_CTSN_M2/FLEXBUS0_CSN_M0/FLEXBUS1_D11/DSMC_RDYN/SAI4_SDI_M1/ETH_CLK0_25M_OUT_M0/VO_EBC_SDSHR/VO_LCDC_D23/GPIO3_A4_d
PWM1_CH1_M3/SPI2_CSN1_M2/UART1_RTSN_M2/FLEXBUS0_D7/DSMC_DATA15/PDM1_SDI3_M2/ETH0_MDIO_M0/VO_EBC_GDSP/VO_LCDC_D22/GPIO3_A5_d
PWM1_CH2_M3/UART10_CTSN_M0/UART1_RX_M2/FLEXBUS0_D6/DSMC_DATA14/PDM1_SDI2_M2/ETH0_MDC_M0/VO_EBC_GDOE/VO_LCDC_D21/GPIO3_A6_d
UART10_RTSN_M0/UART1_TX_M2/FLEXBUS0_D5/DSMC_DATA13/PDM1_CLK1_M2/ETH0_RXCTL_M0/VO_EBC_VCOM/VO_LCDC_D20/GPIO3_A7_d
PWM0_CH0_M3/SPI2_MOSI_M2/UART10_RX_M0/FLEXBUS0_D8/DSMC_CSN1/SAI4_MCLK_M1/ETH0_MCLK_M0/VO_EBC_SDCE3/VO_LCDC_D19/GPIO3_B0_d
PWM1_CH3_M3/SPI4_CSN0_M1/UART10_TX_M0/FLEXBUS0_D4/DSMC_DATA12/PDM1_CLK0_M2/ETH0_RXD1_M0/VO_EBC_SDCE2/VO_LCDC_D18/GPIO3_B1_d
I2C8_SDA_M3/UART9_RX_M1/FLEXBUS0_D3/DSMC_DATA11/PDM1_SDI1_M2/ETH0_RXD0_M0/VO_EBC_SDCE1/VO_LCDC_D17/GPIO3_B2_d
I2C8_SCL_M3/UART9_TX_M1/FLEXBUS0_D2/DSMC_DATA10/PDM1_SDI0_M2/ETH0_TXCTL_M0/VO_EBC_SDCE0/VO_LCDC_D16/GPIO3_B3_d
PWM1_CH4_M3/UART9_RTSN_M1/FLEXBUS0_D1/DSMC_DATA9/SPDIF_RX1_M0/ETH0_TXD1_M0/VO_EBC_SDDO15/VO_LCDC_D15/GPIO3_B4_d
PWM1_CH5_M3/UART9_CTSN_M1/FLEXBUS0_D0/DSMC_DATA8/SPDIF_TX1_M0/ETH0_TXD0_M0/VO_EBC_SDDO14/VO_LCDC_D14/GPIO3_B5_d
PWM0_CH1_M3/SPI3_CSN0_M1/FLEXBUS0_CLK/DSMC_DQS1/ETH0_TXCLK_M0/VO_EBC_SDDO13/VO_LCDC_D13/GPIO3_B6_d
I2C4_SDA_M3/UART3_CTSN_M1/UART2_RX_M2/FLEXBUS1_CSN_M0/FLEXBUS1_D10/DSMC_DQS0/SAI1_SDI0_M1/ETH0_PPSTRIG_M0/VO_EBC_SDDO12/VO_LCDC_D12/GPIO3_B7_d
I2C4_SCL_M3/UART3_RTSN_M1/UART2_TX_M2/FLEXBUS1_D9/DSMC_DATA7/SAI1_SDO3_M1/ETH0_PPSCLK_M0/VO_EBC_SDDO11/VO_LCDC_D11/GPIO3_C0_d
CAN0_RX_M3/I2C5_SDA_M3/SPI4_MISO_M2/UART11_RX_M0/FLEXBUS1_D8/DSMC_DATA6/SAI1_SDO2_M1/ETH0_PPS_REFCLK_M0/VO_EBC_SDDO10/VO_LCDC_D10/GPIO3_C1_d
PWM2_CH0_M3/I2C5_SCL_M3/SPI4_MISO_M1/UART11_RTSN_M0/FLEXBUS0_D7/DSMC_INT1/SAI2_SCLK_M2/ETH0_TXD3_M0/VO_EBC_SDDO9/VO_LCDC_D9/GPIO3_C2_d
PWM2_CH1_M3/I2C5_SDA_M3/SPI4_MOSI_M1/UART11_CTSN_M0/FLEXBUS0_CSN_M2/FLEXBUS0_D6/DSMC_INT3/SAI2_LRCK_M2/ETH0_TXD2_M0/VO_EBC_SDDO8/VO_LCDC_D8/GPIO3_C3_d
CAN0_TX_M3/I2C5_SCL_M3/SPI4_CSN0_M2/UART11_TX_M0/FLEXBUS1_D7/DSMC_DATA5/SAI1_SDO1_M1/VO_EBC_SDDO7/VO_LCDC_D7/GPIO3_C4_d
PWM2_CH2_M3/SPI1_MISO_M2/UART8_RX_M0/FLEXBUS1_D6/DSMC_DATA4/SAI1_SDO0_M1/VO_EBC_SDDO6/VO_LCDC_D6/GPIO3_C5_d
SPI1_MOSI_M2/UART8_TX_M0/FLEXBUS1_D5/DSMC_DATA3/SAI1_LRCK_M1/VO_EBC_SDDO5/VO_LCDC_D5/GPIO3_C6_d
SPI1_CLK_M2/UART8_RTSN_M0/FLEXBUS1_D4/DSMC_DATA2/SAI1_SCLK_M1/VO_EBC_SDDO4/VO_LCDC_D4/GPIO3_C7_d
PWM2_CH3_M3/SPI1_CSN0_M2/UART8_CTSN_M0/FLEXBUS1_D3/DSMC_DATA1/SAI1_MCLK_M1/VO_EBC_SDDO3/VO_LCDC_D3/GPIO3_D0_d
I3C1_SDA_F0_M2/SPI4_CLK_M1/FLEXBUS1_CSN_M2/FLEXBUS0_D1/DSMC_CSN2/SAI2_MCLK_M2/ETH0_RXCLK_M0/VO_EBC_SDDO2/VO_LCDC_D2/GPIO3_D1_d
PWM2_CH4_M3/I3C1_SDA_M2/SPI4_CSN1_M1/UART2_RTSN_M2/FLEXBUS0_CSN_M3/FLEXBUS1_D13_M0/FLEXBUS0_D12/DSMC_CSN3/SAI2_SDI_M2/ETH0_RXD3_M0/VO_EBC_SDDO1/VO_LCDC_D1/GPIO3_D2_d
PWM2_CH5_M3/I3C1_SCL_M2/UART2_CTSN_M2/FLEXBUS1_D2/DSMC_CSN0/SAI2_SDO_M2/ETH0_RXD2_M0/VO_EBC_SDDO0/VO_LCDC_D0/GPIO3_D3_d
I2C9_SCL_M2/SPI3_CLK_M1/UART5_RX_M0/FLEXBUS1_D1/DSMC_DATA0/SAI1_SDI1_M1/VO_EBC_SDLE/VO_LCDC_DEN/GPIO3_D4_d
I2C9_SDA_M2/SPI3_MISO_M1/UART5_TX_M0/FLEXBUS1_D0/DSMC_CLKP/SAI1_SDI2_M1/VO_EBC_GDCLK/VO_LCDC_HSYNC/GPIO3_D5_d
PWM2_CH6_M3/SPI3_MOSI_M1/UART5_CTSN_M0/FLEXBUS1_CLK/DSMC_CLKN/SAI1_SDI3_M1/VO_EBC_SDCLK/VO_LCDC_VSYNC/GPIO3_D6_d
PWM2_CH7_M3/SPI3_CSN1_M1/UART5_RTSN_M0/FLEXBUS1_CSN_M1/FLEXBUS1_D12_M0/FLEXBUS0_D15_M0/DSMC_RESETN/SAI4_SCLK_M1/CAM_CLK0_OUT_M0/VO_EBC_SDOE/VO_LCDC_CLK/GPIO3_D7_d
MIPI_TE_M2/I2C7_SCL_M2/SPI1_CSN1_M2/UART3_TX_M1/FLEXBUS1_CSN_M3/FLEXBUS1_D14_M0/FLEXBUS0_D13_M0/DSMC_INT0/SAI4_LRCK_M1/CAM_CLK1_OUT_M0/SPDIF_RX0_M1/GPIO4_A0_d
I2C7_SDA_M2/UART3_RX_M1/FLEXBUS0_CSN_M1/FLEXBUS1_D13_M0/FLEXBUS0_D14_M0/DSMC_INT2/SAI4_SDO_M1/CAM_CLK2_OUT_M0/SPDIF_TX0_M1/VO_POST_EMPTY/GPIO4_A1_d

1D13 GPIO3_A4
A9
1A7 GPIO3_A6
B13
B14
1A11
A13
A11
B10
1A9
B11
1D12
1E9
1B10
B9
1A8
1D9
1B9
1D7
1C7
1C12
1A12
1A10
B12
1E12
1D10
1C10
1E7
1B12
1B7

ETH_CLK0_25M_OUT_M0 [18]
GMAC0_MDIO_M0 [18]
GMAC0_MDC_M0 [18]
GMAC0_RXCTL_M0 [18]
MIPI_DPHY_CSI_CAM1_PDN_H [19]
GMAC0_RXD1_M0 [18]
GMAC0_RXD0_M0 [18]
GMAC0_TXCTL_M0 [18]
GMAC0_TXD1_M0 [18]
GMAC0_TXD0_M0 [18]
GMAC0_TXCLK_M0 [18]
I2C4_SDA_M3_MIPI_CAM2 [19]
I2C4_SCL_M3_MIPI_CAM2 [19]
I2C5_SDA_M3_MIPI_CAM1 [19]
GMAC0_TXD3_M0 [18]
GMAC0_TXD2_M0 [18]
I2C5_SCL_M3_MIPI_CAM1 [19]
GMAC0_RXCLK_M0 [18]
GMAC0_RXD3_M0 [18]
GMAC0_RXD2_M0 [18]
MIPI_DPHY_CSI_CAM2_PDN_H [19]
MIPI_DPHY_CSI_CAM2_RST_H [19]
CAM1_CLK1_OUT_M0_1V8 [19]

VCCIO5_VCC_0 2A4
VCCIO5_VCC_1 2A5

C1902 NC/100nF X5R 6.3V C0201
C1903 1uF X5R 6.3V C0201
VCC_1V8_S0

VCC_1V8_S0
R1926 2.2K R0201
R1927 2.2K R0201
I2C4_SDA_M3_MIPI_CAM2
I2C4_SCL_M3_MIPI_CAM2

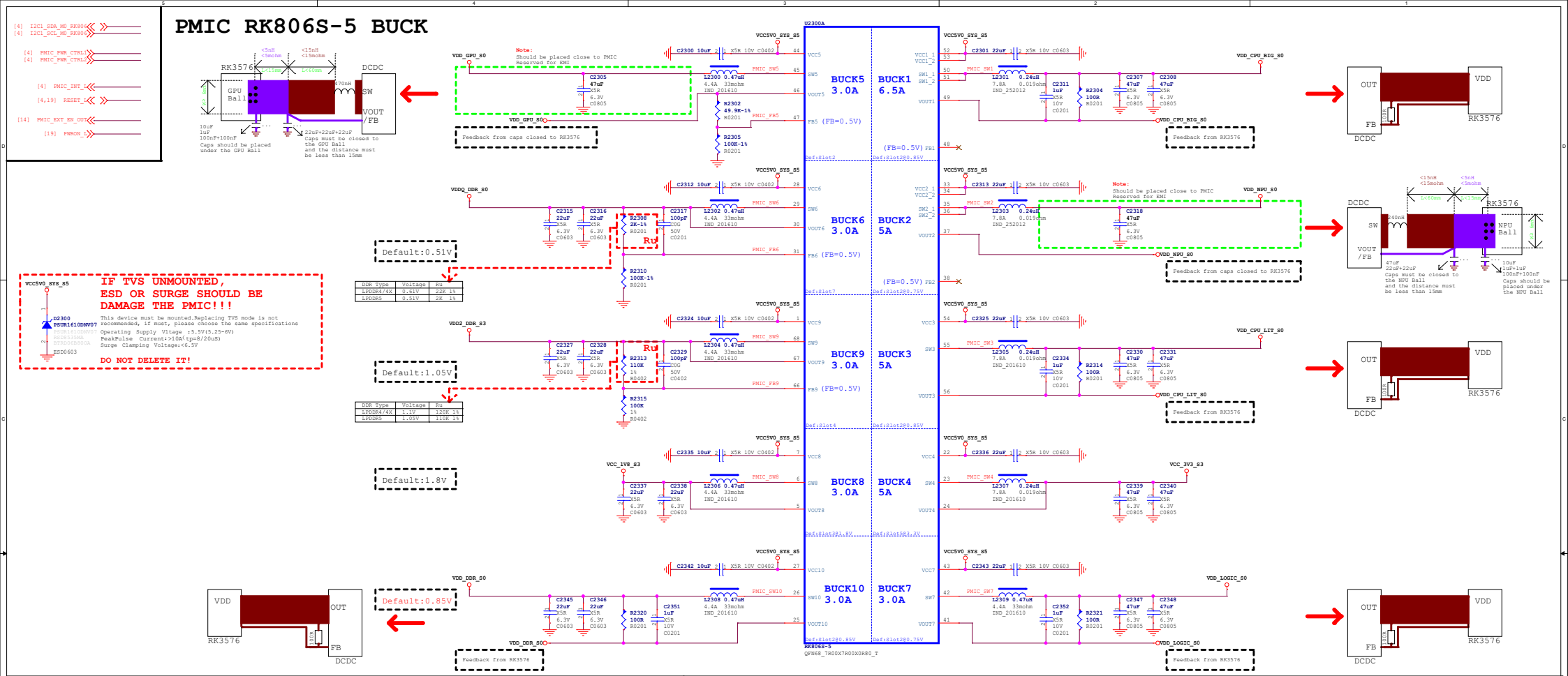
VCC_1V8_S0
R1934 2.2K R0201
R1935 2.2K R0201
I2C5_SDA_M3_MIPI_CAM1
I2C5_SCL_M3_MIPI_CAM1

U1000I
RK3576
BGA698_16R1x17R2x1R18

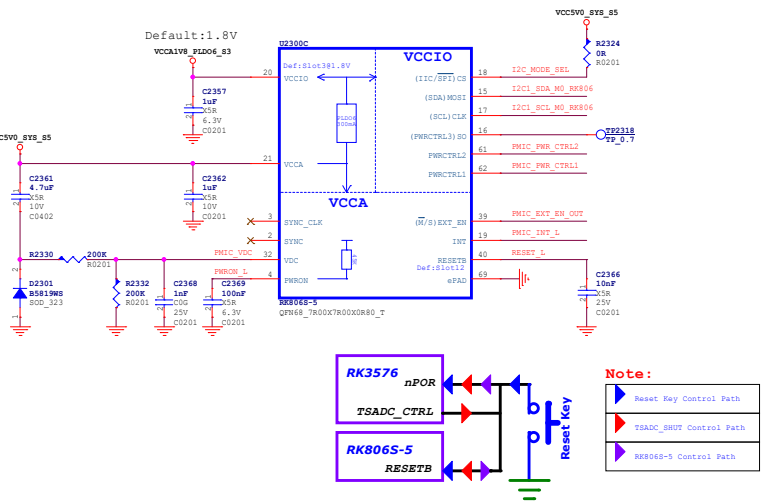
Note:
Caps of between dashed red lines and U1000 should be placed under the U1000 package. Other caps should be placed close to the U1000 package

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	RK3576-GPIO VCCIO4/5				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	12 of 20

PMIC RK806S-5 BUCK

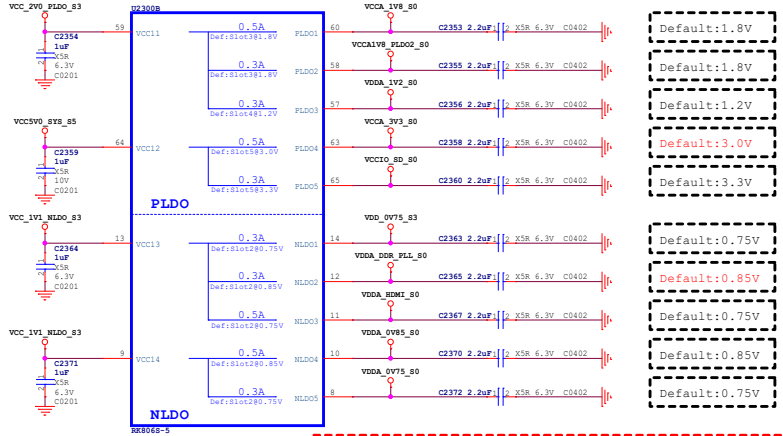


PMIC RK806S-5 Managerment



Note:
I2C Mode:CS(pin18) connected to VCCA(pin21);
SPI Mode(Def):CS(pin18) floating or connected to GND

PMIC RK806S-5 LDO



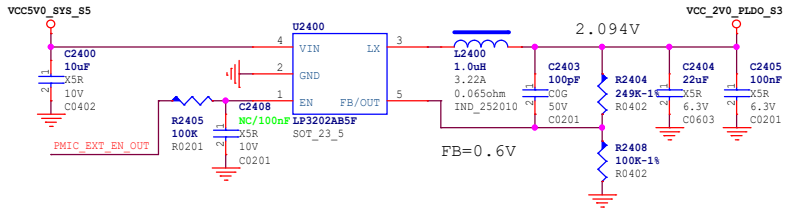
Note:

The RK806 LDO power distribution of the reference chematics is only suitable for the interface used in the reference schematics.
If other interface functions are to be added to the reference schematics, the RK806 LDO distribution needs to be re evaluated, otherwise the added functions may exceed the maximum current provided by the LDO

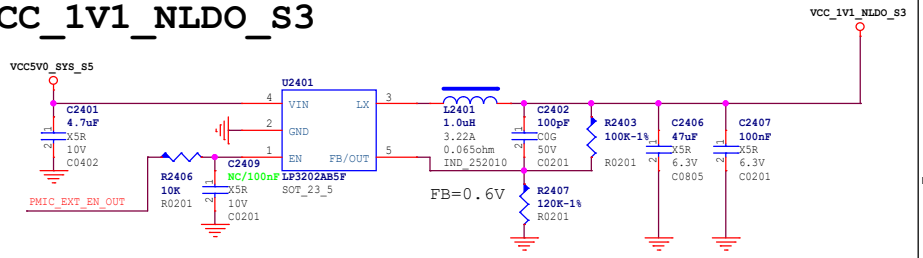
armsom	https://armsom.org/		
Project:	ARMSOM-CM5		
File:	Power-PMIC RK806S-5		
Date:	Tuesday, September 30, 2025	Rev.	V1.3
Designed by:	Park	Reviewed by: <Checker>	Sheet: 13 of 20

[4] I2C2_SCL_M0_CC_RTC
[4] I2C2_SDA_M0_CC_RTC
[4] RTC_INT_L
[4] 32KOUT_RTC2SOC
[17] 32KOUT_RTC2WIFI
[13] PMIC_EXT_EN_OUT
[13,19] PWRON_L

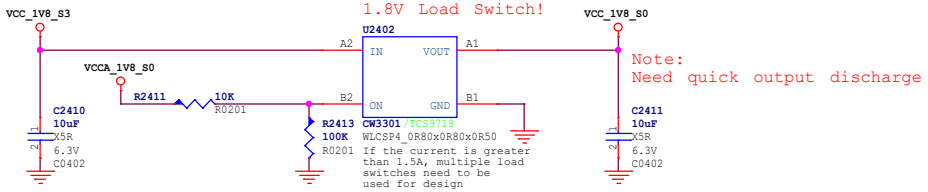
VCC_2V0_PLDO_S3



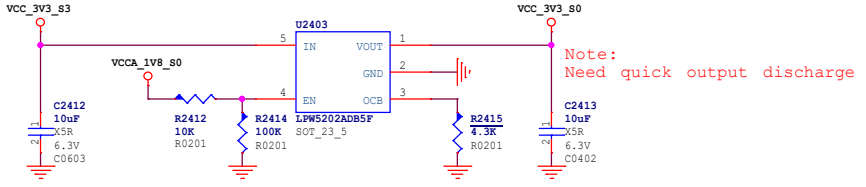
VCC_1V1_NLDO_S3



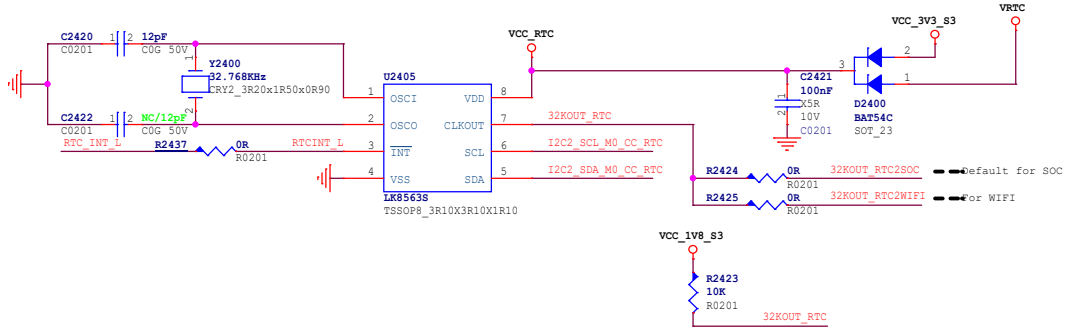
VCC_1V8_S0



VCC_3V3_S0



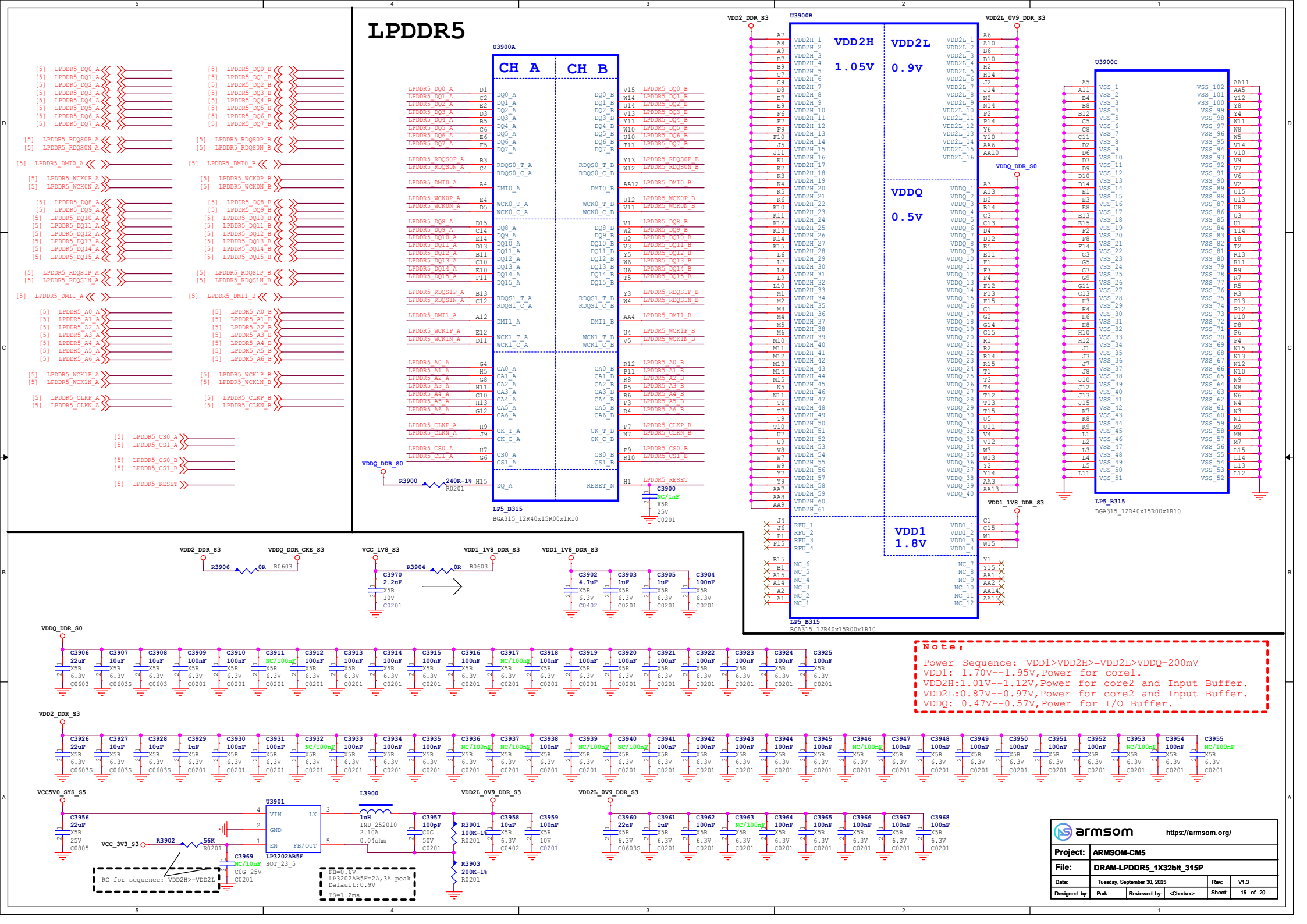
RTC



armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	Power-Ext Discrete/RTC IC				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	14 of 20

LPDDR5

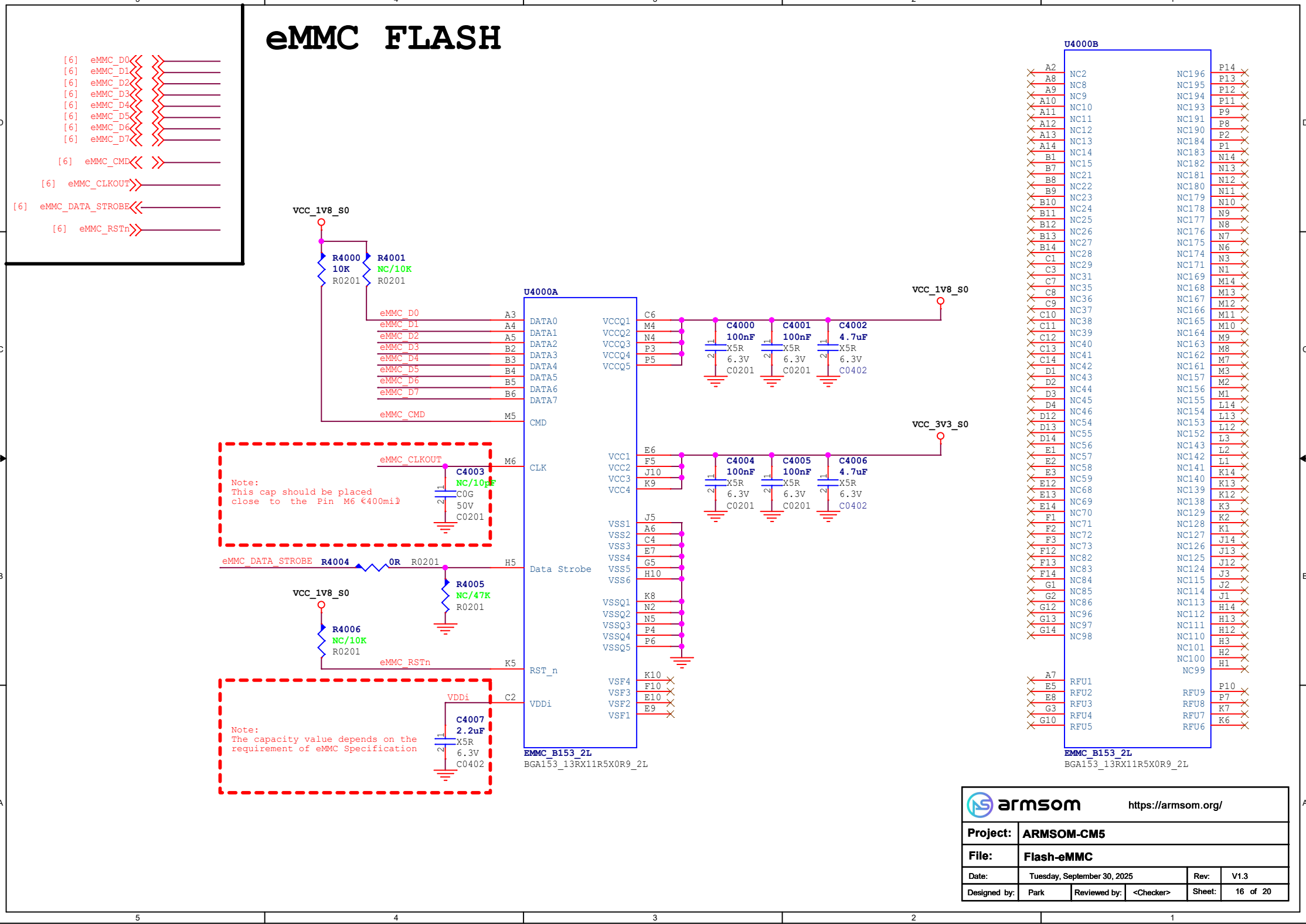


Note:

Power Sequence: VDD1>VDD2H>=VDD2L>VDDQ-200mV
VDD1: 1.70V--1.95V,Power for core1.
VDD2H:1.01V--1.12V,Power for core2 and Input Buffer.
VDD2L:0.87V--0.97V,Power for core2 and Input Buffer.
VDDQ: 0.47V--0.57V,Power for I/O Buffer.

armsom	https://armsom.org/				
Project:	ARMSOM-CM5				
File:	DRAM-LPDDR5_1X32bit_315P				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	15 of 20

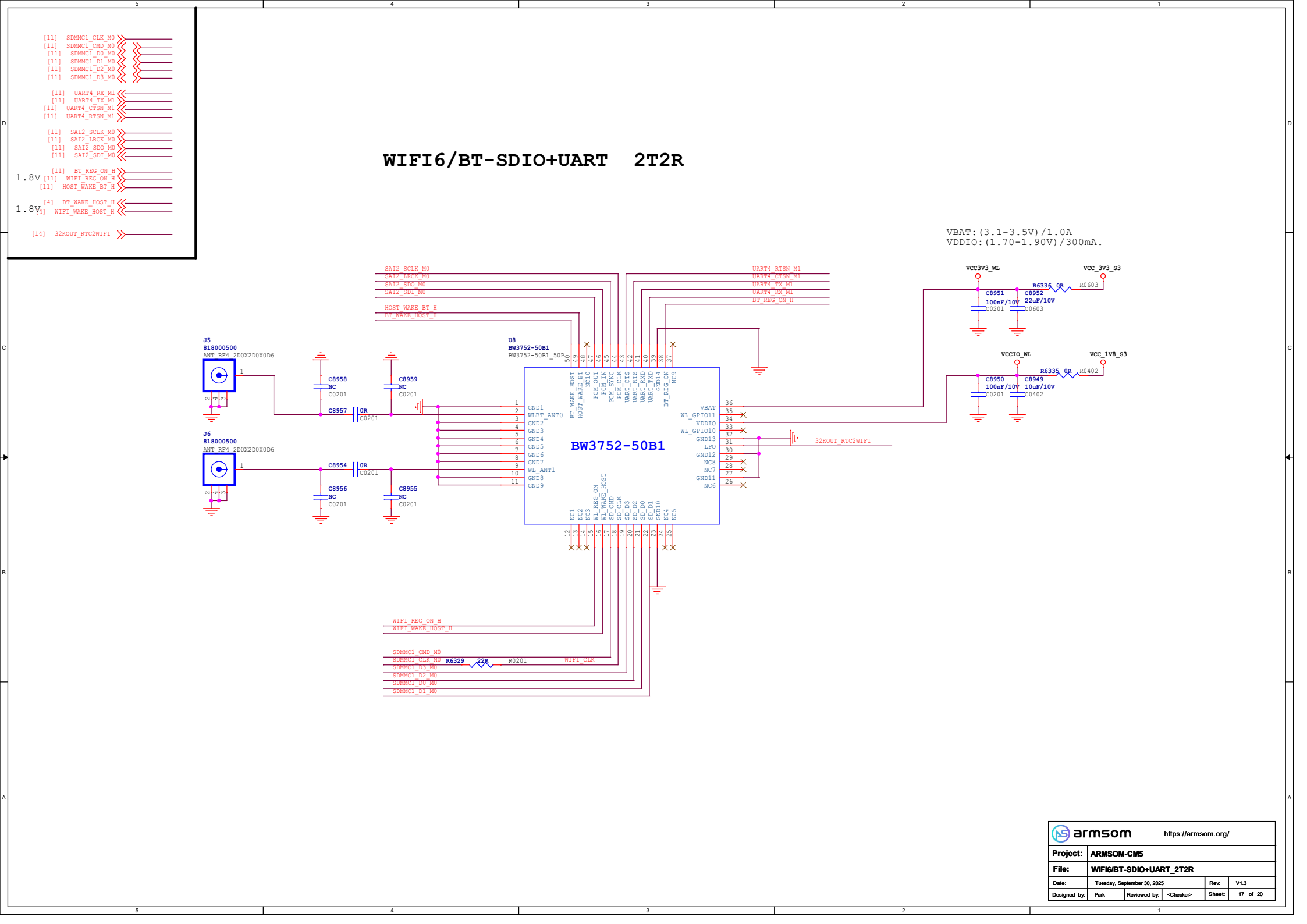
eMMC FLASH



armsom https://armsom.org/

Project:	ARMSOM-CM5				
File:	Flash-eMMC				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 20

WIFI6/BT-SDIO+UART 2T2R



armsom https://armsom.org/					
Project:	ARMSOM-CM5				
File:	WIFI6/BT-SDIO+UART_2T2R				
Date:	Tuesday, September 30, 2025			Rev:	V1.3
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RGMII0_M0

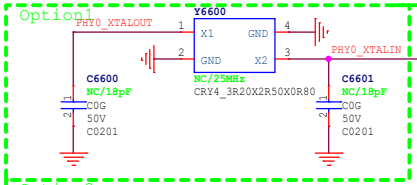
[12] GMAC0_TXD0_M0
[12] GMAC0_TXD1_M0
[12] GMAC0_TXD2_M0
[12] GMAC0_TXD3_M0
[12] GMAC0_TXCTL_M0
[12] GMAC0_TXCLK_M0

[12] GMAC0_RXD0_M0
[12] GMAC0_RXD1_M0
[12] GMAC0_RXD2_M0
[12] GMAC0_RXD3_M0
[12] GMAC0_RXCTL_M0
[12] GMAC0_RXCLK_M0

[12] ETH_CLK0_25M_OUT_M0

[12] GMAC0_MDC_M0
[12] GMAC0_MDIO_M0
[12] GMAC0_RSTn

Option1



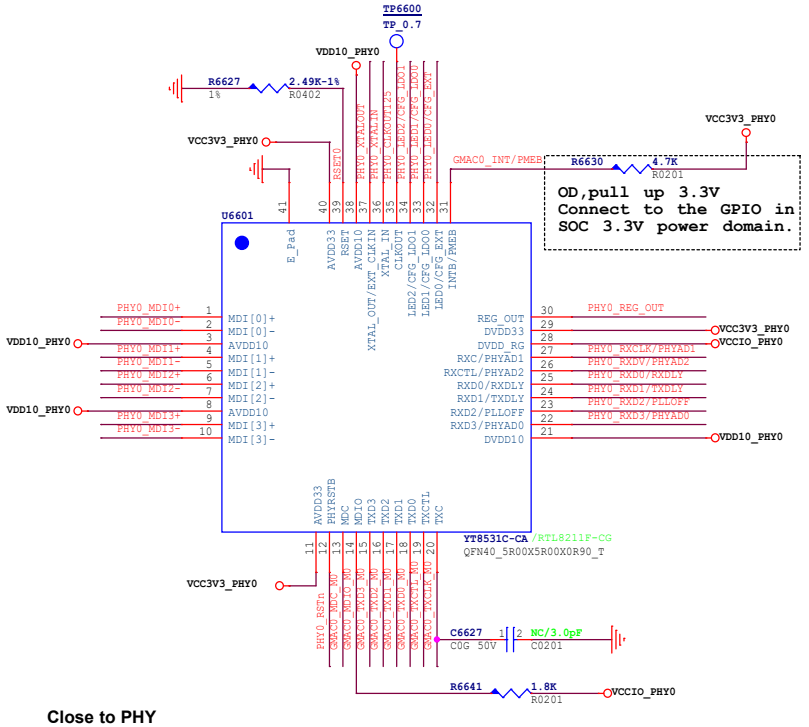
Option2

ETH_CLK0_25M_OUT_M0 R6613 0R R0201 PHY0_XTALOUT

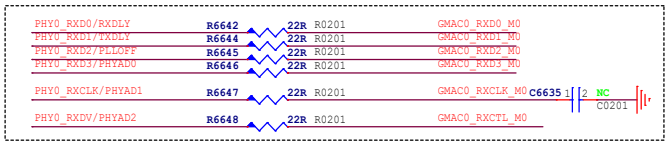
MAC -----> PHY

LAN Interface

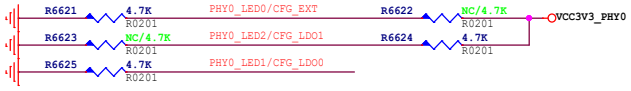
[19] PHY0_MDI3-
[19] PHY0_MDI3+
[19] PHY0_MDI2-
[19] PHY0_MDI2+
[19] PHY0_MDI1-
[19] PHY0_MDI1+
[19] PHY0_MDI0-
[19] PHY0_MDI0+
[19] LAN0_YLED-
[19] LAN0_GLED+



Close to PHY



RGMII Power Source	CFG_EXT	CFG_LDO[1:0]	PHY0_LED2
External 3.3V	1'b1	2'b00	String 510R to GND
External 1.8V	1'b1	2'b10	String 510R to VCC3V3_PHY
Internal 1.8V (default)	1'b0	2'b10	String 510R to VCC3V3_PHY



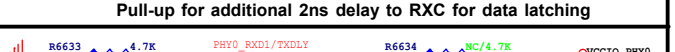
VCC_PHY0_IO Voltage Config



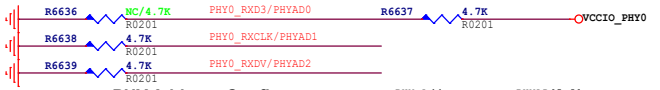
Pull-up to disable PLL @ ALDPS mode(Low power mode)



Pull-up for additional 2ns delay to RXC for data latching

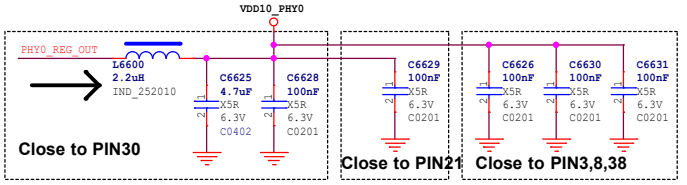


Pull-up for additional 2ns delay to TXC for data latching

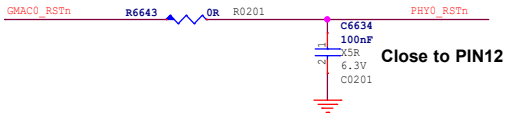


PHY Address Config

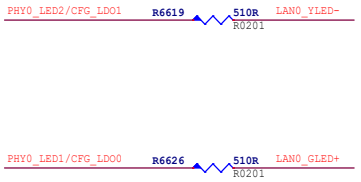
PHY Address	PHYAD[2:0]
1 (default)	3'b001

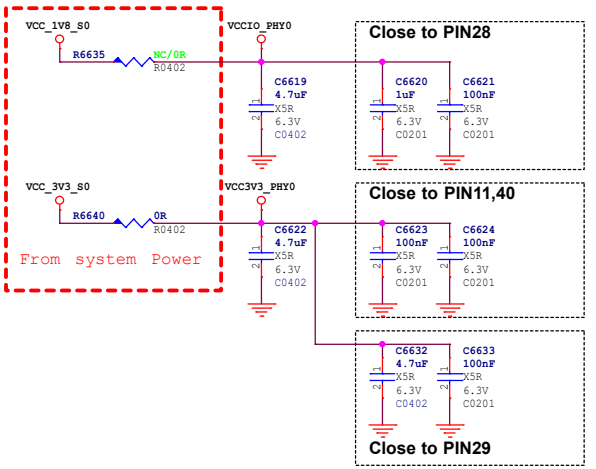


PHYRSTB is 3.3V IO



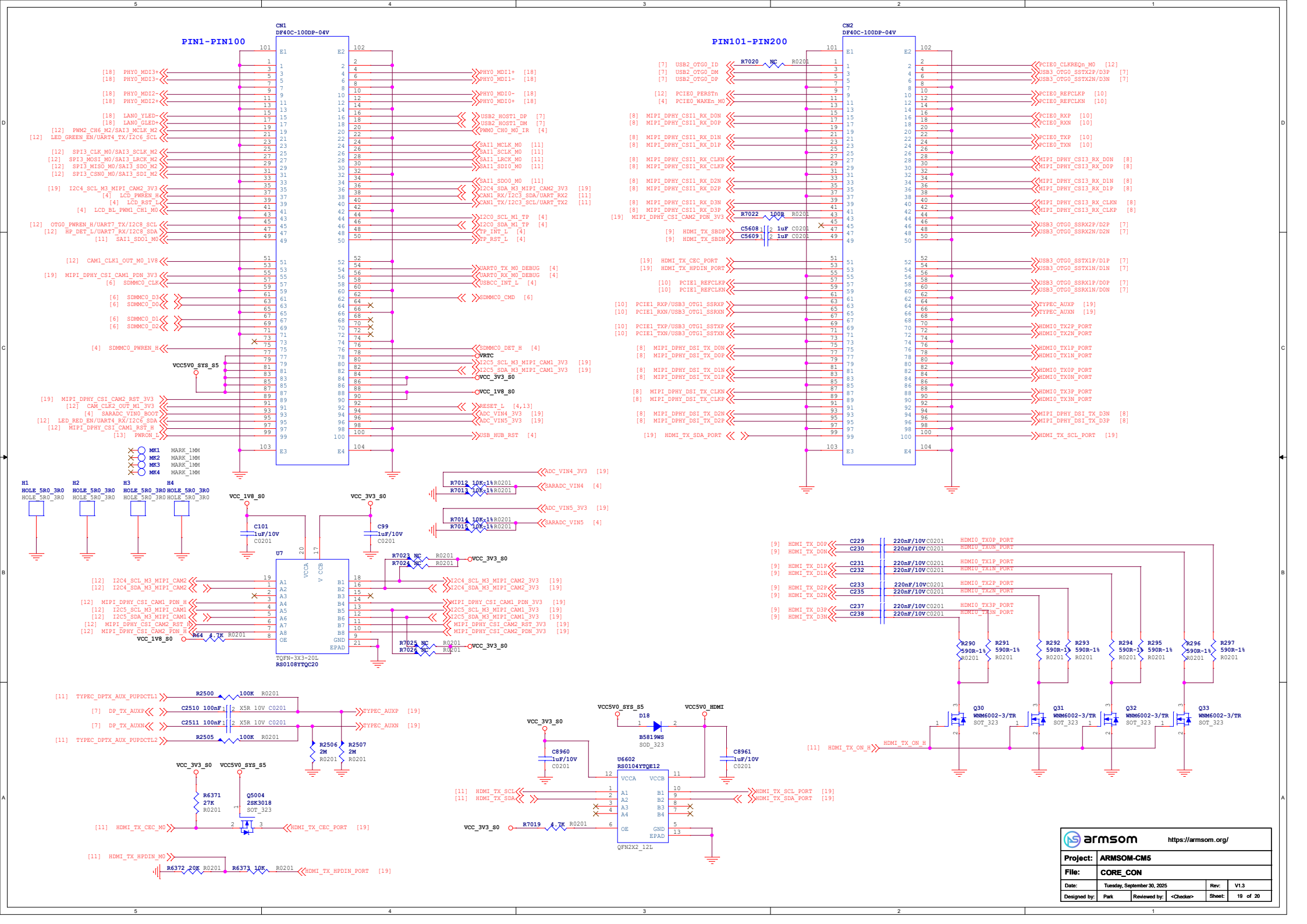
LAN0 LED





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Project:	ARMSOM-CM5				
File:	Ethernet-GEPHY_RGMII0				
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PIN1-PIN100
CN1
DF40C-100DP-04V
PIN101-PIN200
CN2
DF40C-100DP-04V
U7
TQFN-3X3-20L
RS0108YTQC20
U6602
RS0104YTQE12
QFN2X2_12L
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https://armsom.org/
Project: ARMSOM-CM5
File: CORE_CON
Date: Tuesday, September 30, 2025
Rev: V1.3
Designed by: Park
Reviewed by: <Checker>
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Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2024-04-19	Park	1: First version;	
V1.0	2024-05-30	Park	1: del same caps and L3900/L6600 Footprints change to IND_252012 for layout; 2: del wifi module SDIO&I2S series resistors for layout; 3. C3926/C3927/C3928/C3960/C3907 pcbpackge change small for layout; 4. L2305/L2307 pcbpackge change small for layout;	
V1.1	2024-08-27	Park	1.Wifi module=BL-M8852BS2 change to BW3752-50B1; change CN1: pin51&pin91; 2. TF Card_DET: check Low change to Hight; 3. add hdmi circuit to mainboard;	
V1.2	2025-01-20	Park	SARADC_AVDD1V8=VCCA_1V8_S0 change to VCCA1V8_PLDO2_S0;	
V1.3	2025-09-30	Park	change Singal CN1.21:LED_GREEN_EN/UART4_TX/I2C6_SCL;	

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Project:	ARMSOM-CM5				
File:	History				
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