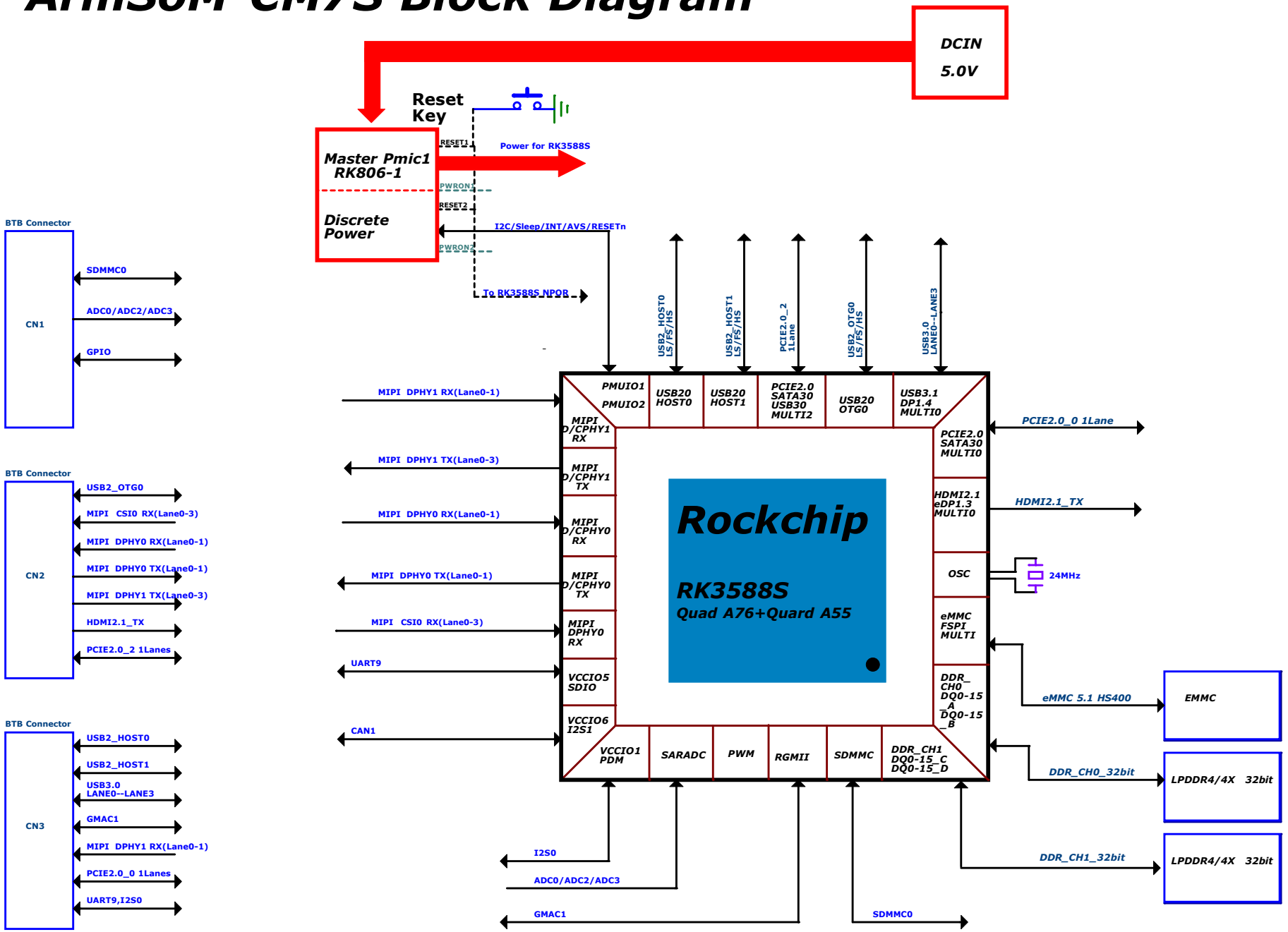
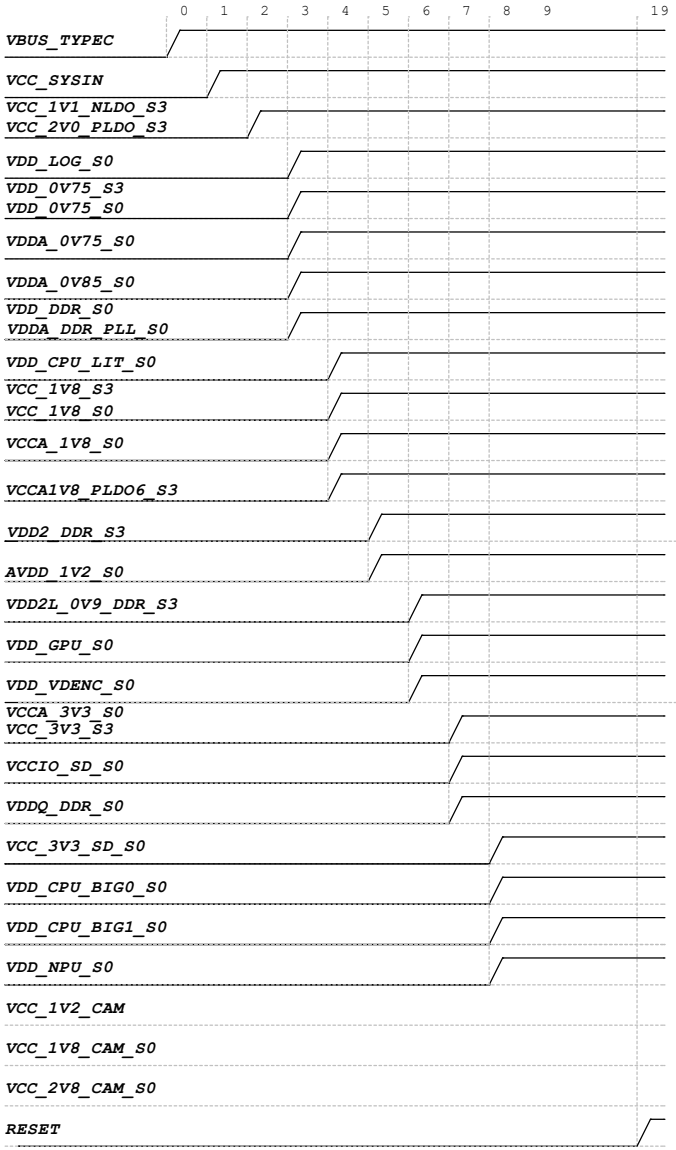
ArmSoM-CM7S Block Diagram



armsom	https://armsom.org/				
Project:	ArmSOM-CM7S				
File:	Block Diagram				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	1 of 18

Power Sequence



Power Supply	PMIC Channel	Supply Limit	Power Name	Time Slot	Default Voltage	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_SYSIN	RK806-1_BUCK1	6.5A	VDD_GPU_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK2	5A	VDD_CPU_LIT_S0	Slot:3	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK3	5A	VDD_LOG_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK4	3A	VDD_VDENC_S0	Slot:5	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK5	2.5A	VDD_DDR_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK6	2.5A	VDD2_DDR_S3	Slot:4	ADJ FB=0.5V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK7	2.5A	VCC_2V0_PLDO_S3	Slot:1	2.0V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK8	2.5A	VCC_3V3_S3	Slot:6	3.3V	ON	ON	TBD	TBD
VCC_SYSIN	RK806-1_BUCK9	2.5A	VDDQ_DDR_S0	Slot:6	ADJ FB=0.5V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_BUCK10	2.5A	VCC_1V8_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_2V0_PLDO_S3	RK806-1_PLDO1	0.5A	VCC_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO2	0.3A	VCCA_1V8_S0	Slot:3	1.8V	ON	OFF	TBD	TBD
	RK806-1_PLDO3	0.3A	VDDA_1V2_S0	Slot:4	1.2V	ON	OFF	TBD	TBD
VCC_SYSIN	RK806-1_PLDO4	0.5A	VCCA_3V3_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO5	0.3A	VCCIO_SD_S0	Slot:6	3.3V	ON	OFF	TBD	TBD
	RK806-1_PLDO6	0.3A	VCCA1V8_PLDO6_S3	Slot:3	1.8V	ON	ON	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO1	0.3A	VDD_0V75_S3	Slot:2	0.75V	ON	ON	TBD	TBD
	RK806-1_NLDO2	0.3A	VDDA_DDR_PLL_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO3	0.5A	VDDA_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_1V1_NLDO_S3	RK806-1_NLDO4	0.5A	VDDA_0V85_S0	Slot:2	0.85V	ON	OFF	TBD	TBD
	RK806-1_NLDO5	0.3A	VDD_0V75_S0	Slot:2	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_CPU_BIG0_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-3	6A	VDD_CPU_BIG1_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	BUCK_RK860-2	6A	VDD_NPU_S0	Slot:6A	0.75V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VCC_1V1_NLDO_S3	Slot:1	1.1V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2A	VDD2L_0V9_DDR_S3	Slot:5	0.9V	ON	ON	TBD	TBD
VCC_SYSIN	EXT BUCK	2.5A	VCC_3V3_SD_S0	Slot:6A	3.3V	ON	OFF	TBD	TBD
VCC_SYSIN	EXT_BUCK or LDO	2A	VCC_1V2_CAM_S0	OFF	1.2V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_1V8_CAM_S0	OFF	1.8V	OFF	OFF	TBD	TBD
VCC_SYSIN	LDO	0.5A	VCC_2V8_CAM_S0	OFF	2.8V	OFF	OFF	TBD	TBD

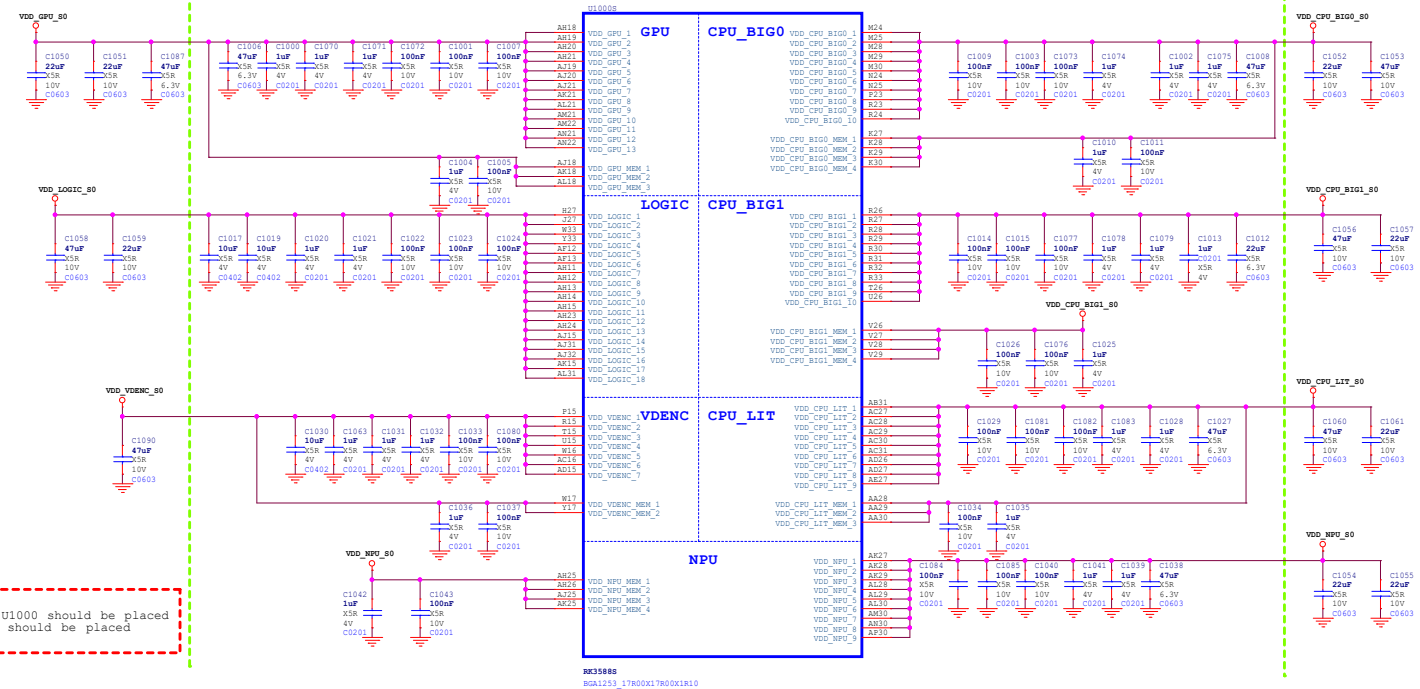
IO Power Domain Map

IO Domain	Pin Num	Support IO Voltage	Supply Power Pin Name	Power Source	Operating Voltage
PMUIO1	Pin N36 N37	1.8V Only	PMUIO1_1V8	VCC_1V8_S3	1.8V
PMUIO2	Pin V37 Y37 Pin V35 V36	1.8V or 3.3V	PMUIO2_1V8 PMUIO2	VCC_1V8_S3 VCC_1V8_S3	1.8V 1.8V
EMMCIO	Pin AC35 Pin AC36	1.8V Only	EMMCIO_1V8	VCC_1V8_S0	1.8V
VCCIO1	Pin H31	1.8V Only	VCCIO1_1V8	VCC_1V8_S0	1.8V
VCCIO2	Pin AK11 Pin AK10	1.8V or 3.3V	VCCIO2_1V8 VCCIO2	VCC_1V8_S0 VCC_IO_SD	1.8V 1.8V/3.3V
VCCIO4	Pin G27 G28 Pin G31	1.8V or 3.3V	VCCIO4_1V8 VCCIO4	VCC_1V8_S0 VCC_3V3_S0	1.8V 1.8V
VCCIO5	Pin AF35 AF36 Pin AC33 AC34	1.8V or 3.3V	VCCIO5_1V8 VCCIO5	VCC_1V8_S0 VCC_1V8_S0	1.8V 1.8V
VCCIO6	Pin AJ34 Pin AL33 AM33	1.8V or 3.3V	VCCIO6_1V8 VCCIO6	VCC_1V8_S0 VCC_3V3_S0	1.8V 3.3V

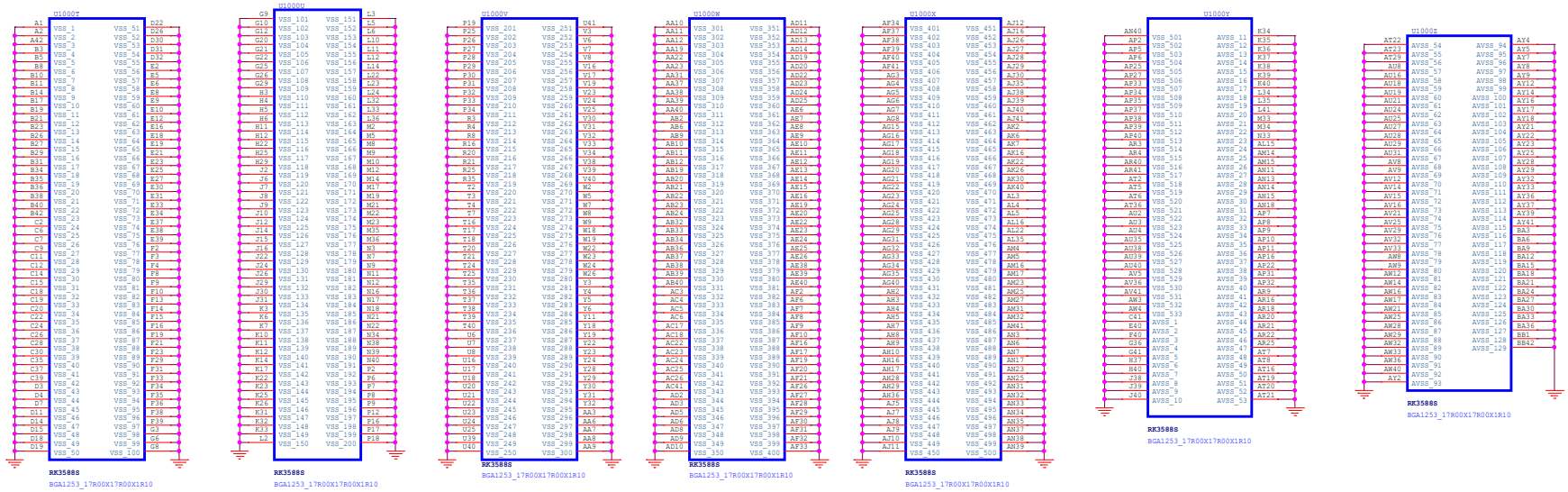
armsom https://armsom.org/

Project:	ArmSOM-CM7S				
File:	System Power Sequence				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	2 of 18

RK3588S(Power&Gnd)



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



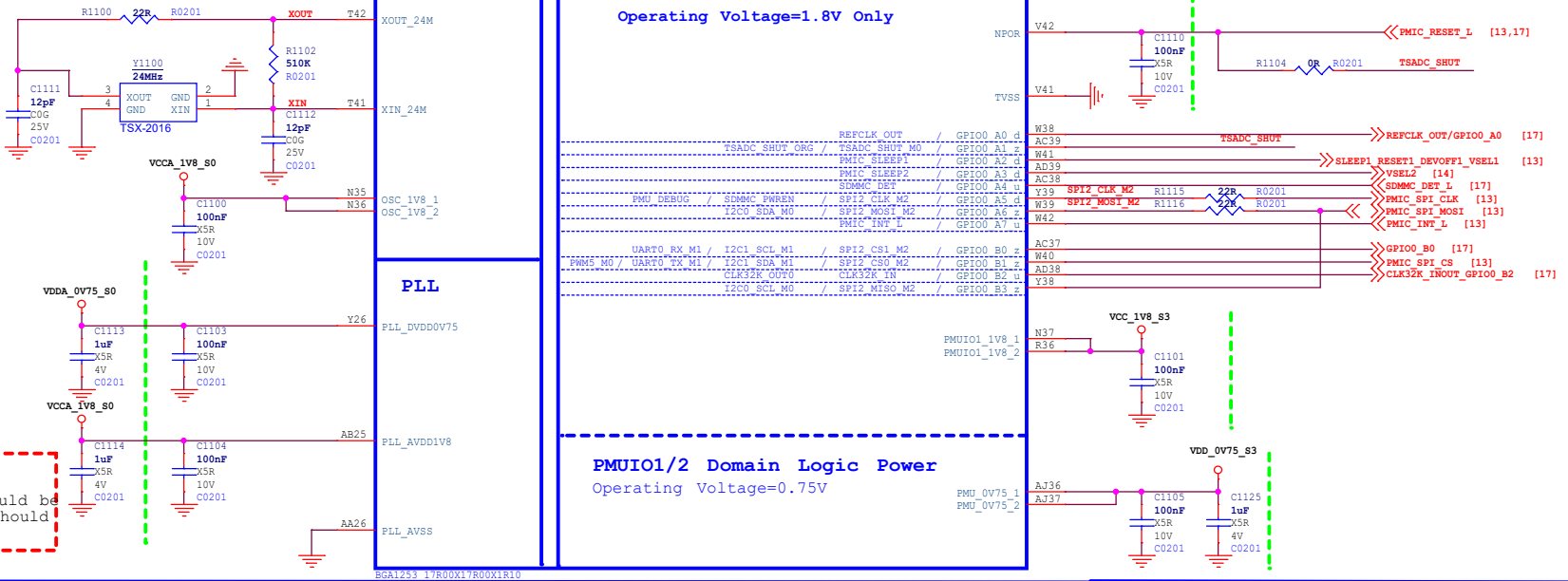
armsom	https://armsom.org/
Project:	ArmSOM-CM7S
File:	RK3588S_Power/GND
Date:	Thursday, July 23, 2026
Rev:	V1.2
Designed by:	Park
Reviewed by:	<Checker>
Sheet:	3 of 18

RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

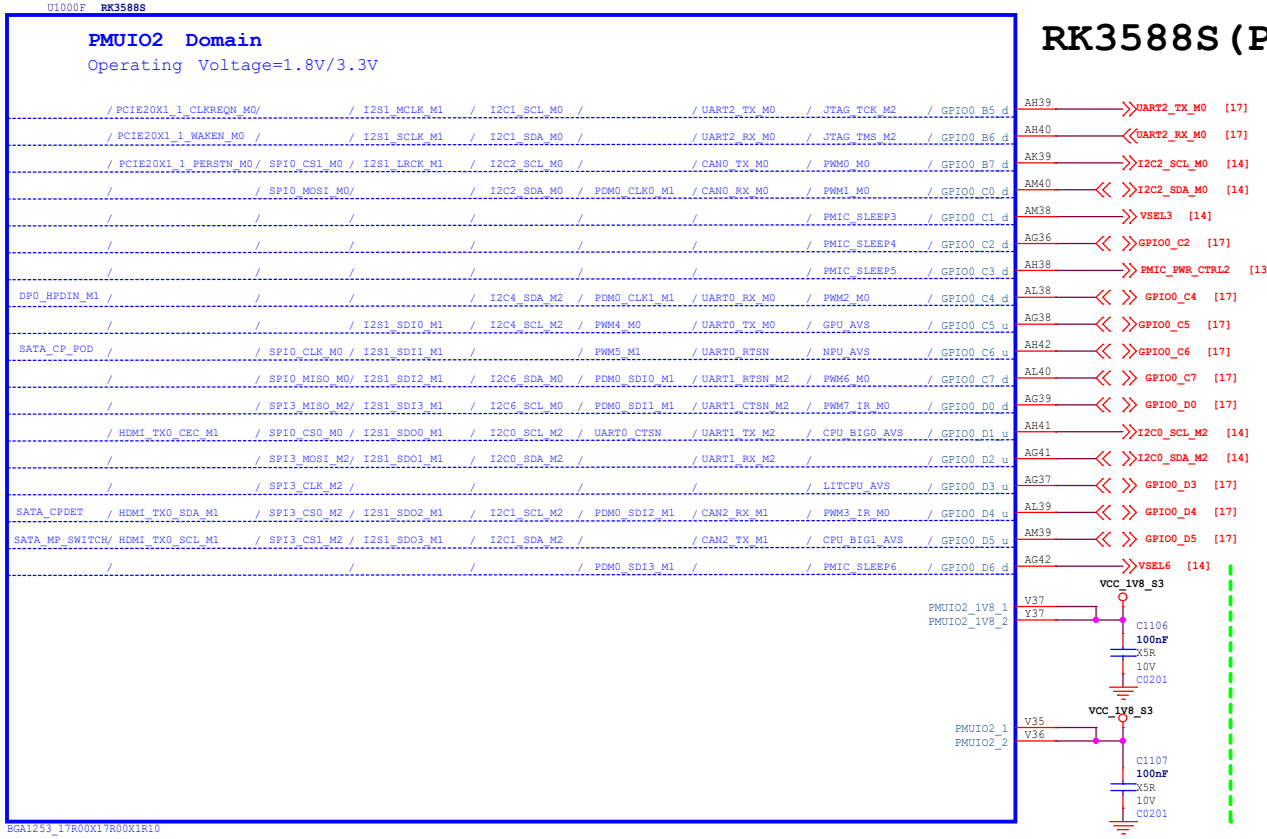
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



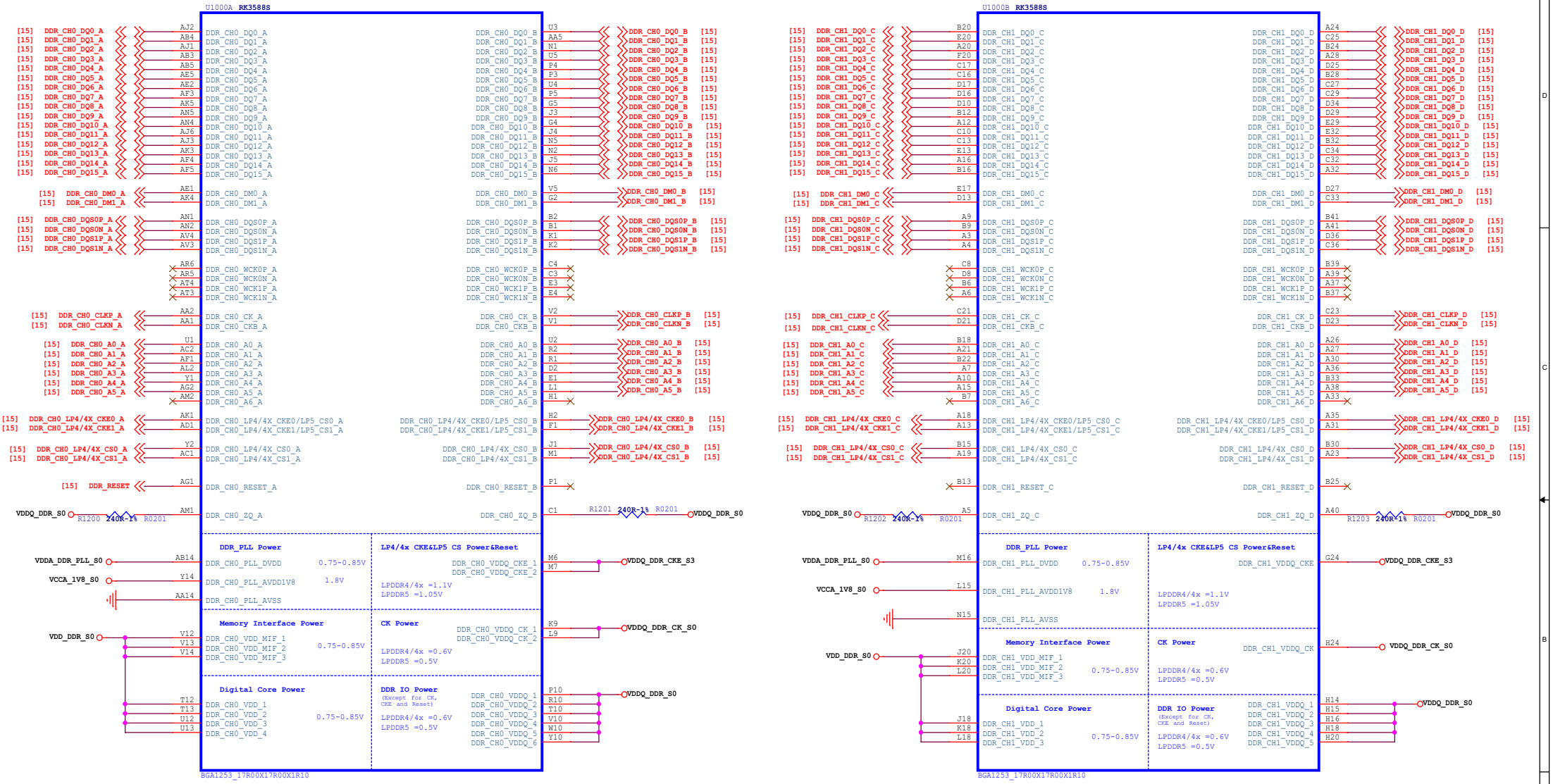
Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

RK3588S(PMUIO2)

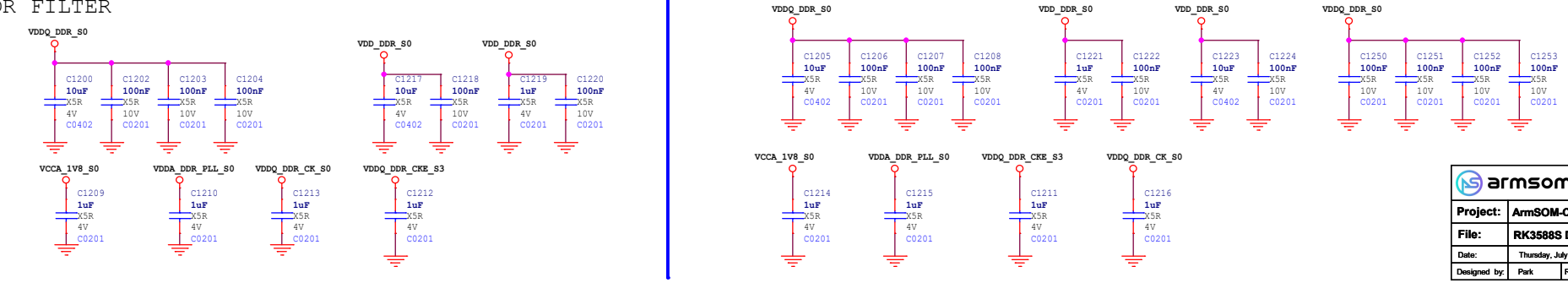


armsom	https://armsom.org/				
Project:	ArmSOM-CM7S				
File:	RK3588S_OSC/PLL/PMUIO				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	4 of 18

RK3588S(DDR PHY)

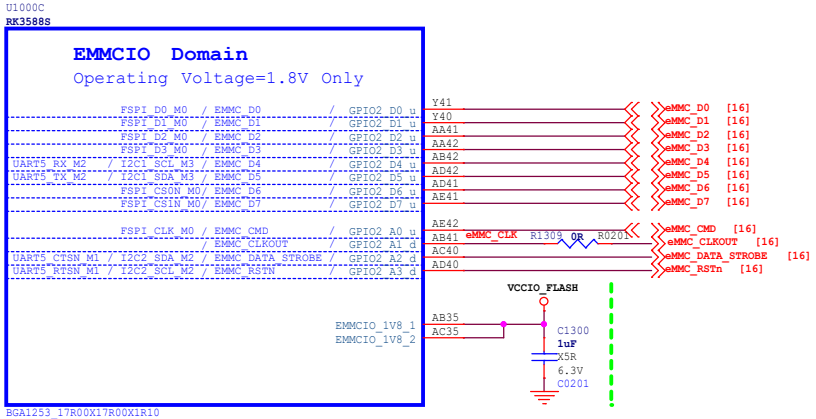


DDR FILTER

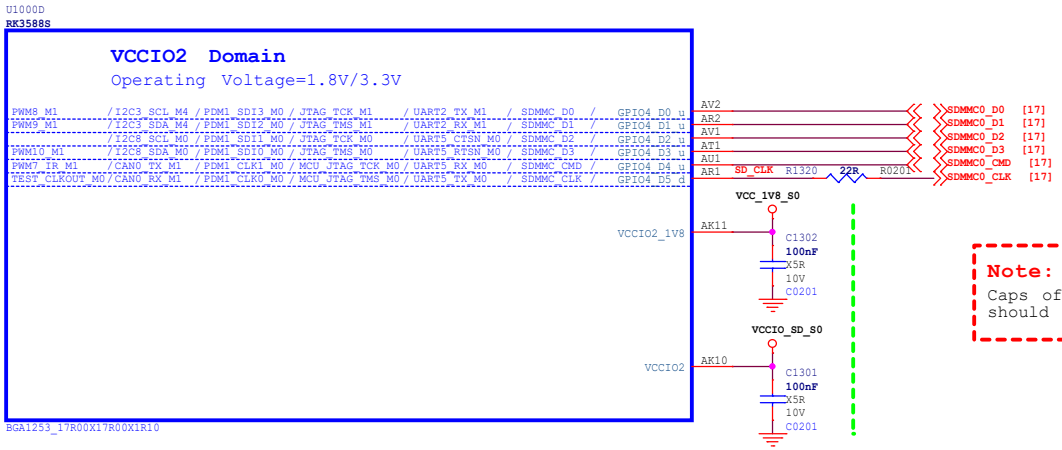


armsom	https://armsom.org/		
Project:	ArmSOM-CM7S		
File:	RK3588S DDR Controller		
Date:	Thursday, July 23, 2026	Rev:	V1.2
Designed by: Park	Reviewed by: <Checker>	Sheet:	5 of 18

RK3588S(EMMCIO Domain)



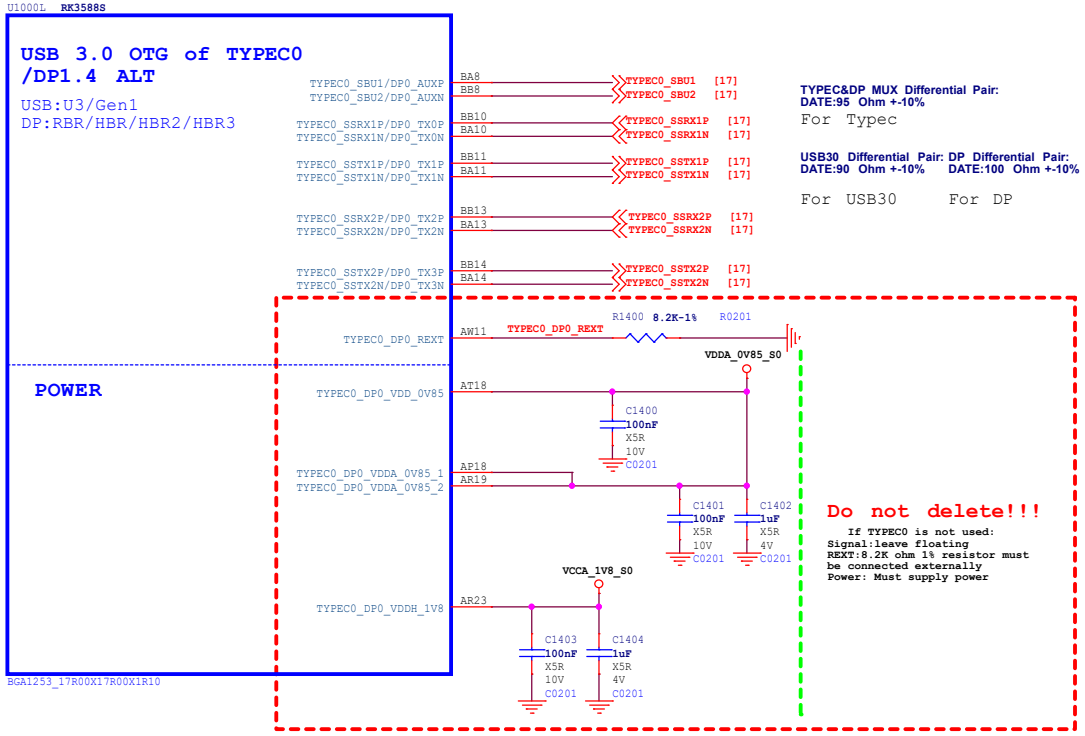
RK3588S(VCCIO2 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom https://armsom.org/					
Project:	ArmSOM-CM7S				
File:	RK3588S Flash/SD Controller				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	6 of 18

RK3588S(USB3.0/DP1.4)

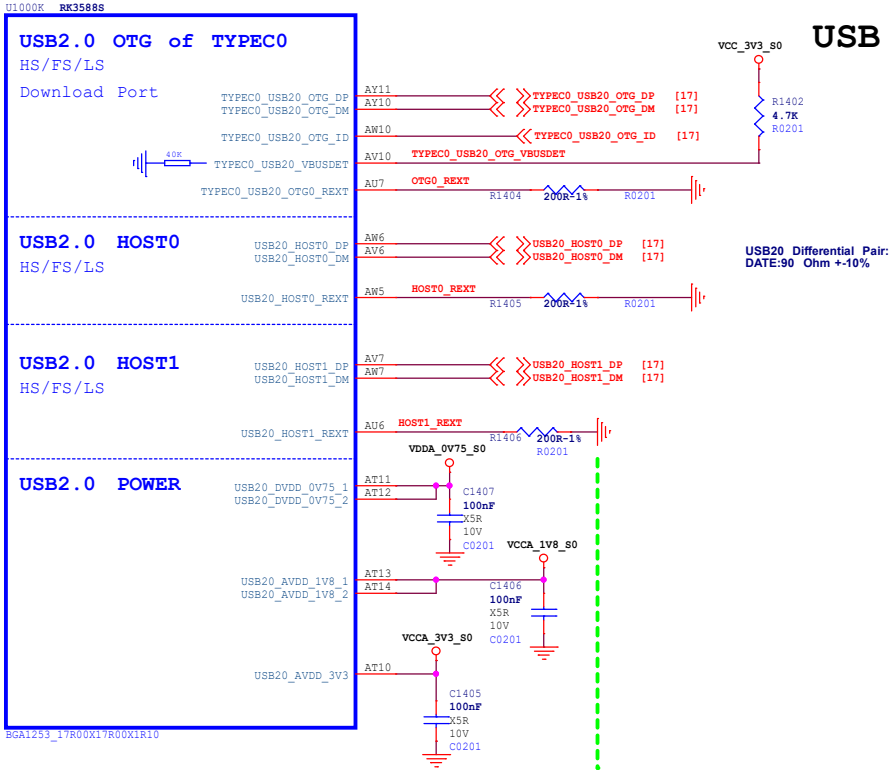


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



USB Detection

Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

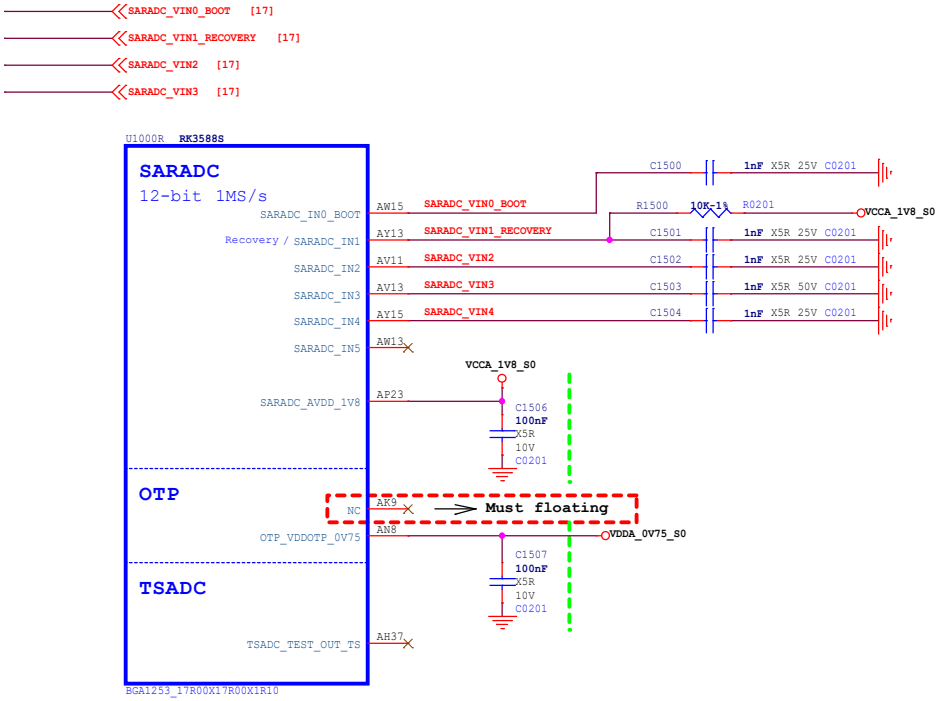
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

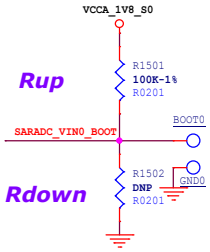
armsom https://armsom.org/

Project:	ArmSOM-CM7S				
File:	RK3588S_USB20/USB30/DP PHY				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	7 of 18

RK3588S(SARADC/OTP/TSADC)

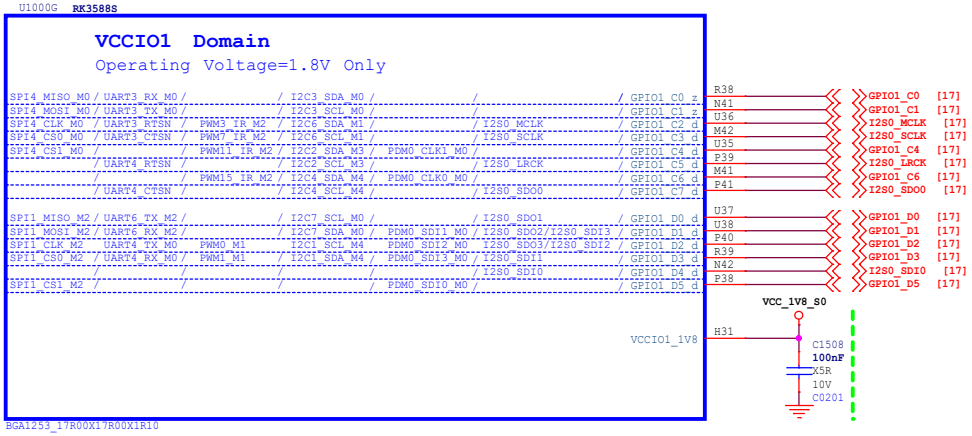


BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

RK3588S(VCCIO1 Domain)



Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom https://armsom.org/

Project:	ArmSOM-CM7S				
File:	RK3588S_SARADC/1.8V GPIO				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	8 of 18

RK3588S(MIPI_CSI)

U1000N

MIPI DPHY CSI_RX Port0

MIPI V1.2
2.5Gbps

MIPI_CSI0_CLK0P	AN42	MIPI_CSI0_RX_CLK0P [17]
MIPI_CSI0_CLK0N	AN41	MIPI_CSI0_RX_CLK0N [17]
MIPI_CSI0_D0P	AL42	MIPI_CSI0_RX_D0P [17]
MIPI_CSI0_D0N	AL41	MIPI_CSI0_RX_D0N [17]
MIPI_CSI0_D1P	AK41	MIPI_CSI0_RX_D1P [17]
MIPI_CSI0_D1N	AK42	MIPI_CSI0_RX_D1N [17]
MIPI_CSI0_CLK1P	AU41	MIPI_CSI0_RX_CLK1P [17]
MIPI_CSI0_CLK1N	AU42	MIPI_CSI0_RX_CLK1N [17]
MIPI_CSI0_D2P	AT41	MIPI_CSI0_RX_D2P [17]
MIPI_CSI0_D2N	AT42	MIPI_CSI0_RX_D2N [17]
MIPI_CSI0_D3P	AP42	MIPI_CSI0_RX_D3P [17]
MIPI_CSI0_D3N	AP41	MIPI_CSI0_RX_D3N [17]

MIPI_CSI0_AVCC0V75 — AM37 — VDDA_0V75_S0
- C1602 100nF X5R 10V C0201
- C1603 1uF X5R 4V C0201

MIPI_CSI0_AVCC1V8 — AM35 — VCCA_1V8_S0
- C1600 1uF X5R 4V C0201
- C1601 100nF X5R 10V C0201

RK3588S
BGA1253_17R00X17R00X1R10

MIPI CSI_RX:
100 Ohm ± 10 %

Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3588S(MIPI_D/C PHY)

U1000O

MIPI D/C-PHY DSI_TX Port0

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_TX_CLKP/MIPI_CPHY0_TX_TRIO1_C	BB34	MIPI_DPHY0_TX_CLKP [17]
MIPI_DPHY0_TX_CLKN/MIPI_CPHY0_TX_TRIO1_B	BA34	MIPI_DPHY0_TX_CLKN [17]
MIPI_DPHY0_TX_D0P/MIPI_CPHY0_TX_TRIO0_B	BB31	MIPI_DPHY0_TX_D0P [17]
MIPI_DPHY0_TX_D0N/MIPI_CPHY0_TX_TRIO0_A	BA31	MIPI_DPHY0_TX_D0N [17]
MIPI_DPHY0_TX_D1P/MIPI_CPHY0_TX_TRIO1_A	BA32	MIPI_DPHY0_TX_D1P [17]
MIPI_DPHY0_TX_D1N/MIPI_CPHY0_TX_TRIO0_C	BB32	MIPI_DPHY0_TX_D1N [17]
MIPI_DPHY0_TX_D2P/MIPI_CPHY0_TX_TRIO2_B	BA35	
MIPI_DPHY0_TX_D2N/MIPI_CPHY0_TX_TRIO2_A	BB35	
MIPI_DPHY0_TX_D3P/NO_USE	BB37	
MIPI_DPHY0_TX_D3N/MIPI_CPHY0_TX_TRIO2_C	BA37	

MIPI D/C-PHY CSI_RX Port0

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY0_RX_CLKP/MIPI_CPHY0_RX_TRIO1_C	BB41	MIPI_DPHY0_RX_CLKP [17]
MIPI_DPHY0_RX_CLKN/MIPI_CPHY0_RX_TRIO1_B	BA41	MIPI_DPHY0_RX_CLKN [17]
MIPI_DPHY0_RX_D0P/MIPI_CPHY0_RX_TRIO0_B	BB38	MIPI_DPHY0_RX_D0P [17]
MIPI_DPHY0_RX_D0N/MIPI_CPHY0_RX_TRIO0_A	BA38	MIPI_DPHY0_RX_D0N [17]
MIPI_DPHY0_RX_D1P/MIPI_CPHY0_RX_TRIO1_A	BA40	MIPI_DPHY0_RX_D1P [17]
MIPI_DPHY0_RX_D1N/MIPI_CPHY0_RX_TRIO0_C	AY40	MIPI_DPHY0_RX_D1N [17]
MIPI_DPHY0_RX_D2P/MIPI_CPHY0_RX_TRIO2_B	AY42	
MIPI_DPHY0_RX_D2N/MIPI_CPHY0_RX_TRIO2_A	BA42	
MIPI_DPHY0_RX_D3P/NO_USE	AW41	
MIPI_DPHY0_RX_D3N/MIPI_CPHY0_RX_TRIO2_C	AW42	

Power

MIPI_D/C_PHY0_VREG — AT33 MIPI_D/C_PHY0_VREG — C1604 1uF C0201

MIPI_D/C_PHY0_VDD — AR33 — VDDA_0V75_S0
- C1605 1uF X5R 4V C0201
- C1611 100nF X5R 10V C0201

MIPI_D/C_PHY_VDD_1V2_1 — AR34 — VDDA_1V2_S0
- C1607 100nF X5R 10V C0201

MIPI_D/C_PHY_VDD_1V8_1 — AR30 — VCCA_1V8_S0
- C1609 100nF X5R 10V C0201

RK3588S
BGA1253_17R00X17R00X1R10

MIPI DPHY:
100 Ohm ± 10 %

MIPI CPHY:
50 Ohm ± 10 %

U1000P

MIPI D/C-PHY DSI_TX Port1

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_TX_CLKP/MIPI_CPHY1_TX_TRIO1_C	BB19	MIPI_DPHY1_TX_CLKP [17]
MIPI_DPHY1_TX_CLKN/MIPI_CPHY1_TX_TRIO1_B	BA19	MIPI_DPHY1_TX_CLKN [17]
MIPI_DPHY1_TX_D0P/MIPI_CPHY1_TX_TRIO0_B	BB16	MIPI_DPHY1_TX_D0P [17]
MIPI_DPHY1_TX_D0N/MIPI_CPHY1_TX_TRIO0_A	BA16	MIPI_DPHY1_TX_D0N [17]
MIPI_DPHY1_TX_D1P/MIPI_CPHY1_TX_TRIO1_A	BA17	MIPI_DPHY1_TX_D1P [17]
MIPI_DPHY1_TX_D1N/MIPI_CPHY1_TX_TRIO0_C	BB17	MIPI_DPHY1_TX_D1N [17]
MIPI_DPHY1_TX_D2P/MIPI_CPHY1_TX_TRIO2_B	BA20	MIPI_DPHY1_TX_D2P [17]
MIPI_DPHY1_TX_D2N/MIPI_CPHY1_TX_TRIO2_A	BB20	MIPI_DPHY1_TX_D2N [17]
MIPI_DPHY1_TX_D3P/NO_USE	BB22	MIPI_DPHY1_TX_D3P [17]
MIPI_DPHY1_TX_D3N/MIPI_CPHY1_TX_TRIO2_C	BA22	MIPI_DPHY1_TX_D3N [17]

MIPI D/C-PHY CSI_RX Port1

D-PHY:V2.0
4.5Gbps/Lane

C-PHY:V1.1
5.7Gbps/Trio

MIPI_DPHY1_RX_CLKP/MIPI_CPHY1_RX_TRIO1_C	BA26	MIPI_DPHY1_RX_CLKP [17]
MIPI_DPHY1_RX_CLKN/MIPI_CPHY1_RX_TRIO1_B	BB26	MIPI_DPHY1_RX_CLKN [17]
MIPI_DPHY1_RX_D0P/MIPI_CPHY1_RX_TRIO0_B	BA23	MIPI_DPHY1_RX_D0P [17]
MIPI_DPHY1_RX_D0N/MIPI_CPHY1_RX_TRIO0_A	BB23	MIPI_DPHY1_RX_D0N [17]
MIPI_DPHY1_RX_D1P/MIPI_CPHY1_RX_TRIO1_A	BB25	MIPI_DPHY1_RX_D1P [17]
MIPI_DPHY1_RX_D1N/MIPI_CPHY1_RX_TRIO0_C	BA25	MIPI_DPHY1_RX_D1N [17]
MIPI_DPHY1_RX_D2P/MIPI_CPHY1_RX_TRIO2_B	BB28	
MIPI_DPHY1_RX_D2N/MIPI_CPHY1_RX_TRIO2_A	BA28	
MIPI_DPHY1_RX_D3P/NO_USE	BA29	
MIPI_DPHY1_RX_D3N/MIPI_CPHY1_RX_TRIO2_C	BB29	

Power

MIPI_D/C_PHY1_VREG — AT27 MIPI_D/C_PHY1_VREG — C1612 1uF X5R C0201

MIPI_D/C_PHY1_VDD — AR27 — VDDA_0V75_S0
- C1613 1uF X5R 4V C0201
- C1614 100nF X5R 10V C0201

MIPI_D/C_PHY_VDD_1V2_2 — AR35 — VDDA_1V2_S0
- C1608 100nF X5R 10V C0201

MIPI_D/C_PHY_VDD_1V8_2 — AT30 — VCCA_1V8_S0
- C1610 100nF X5R 10V C0201

RK3588S
BGA1253_17R00X17R00X1R10

armsom https://armsom.org/

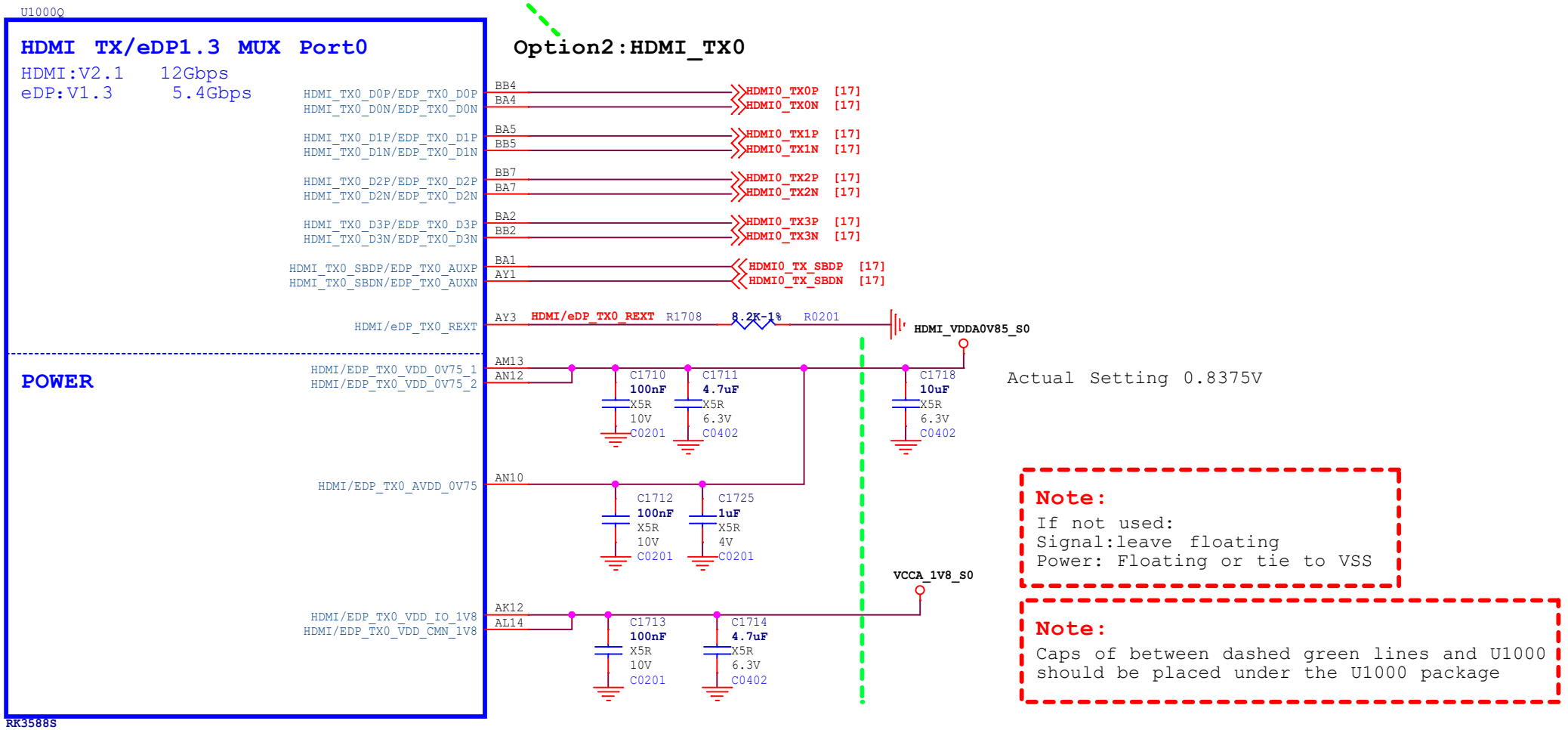
Project:	ArmSOM-CM7S				
File:	RK3588S_MIPI Interface				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	9 of 18

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

HDMI TX
100 Ohm ± 10 %

eDP TX
100 Ohm ± 10 %

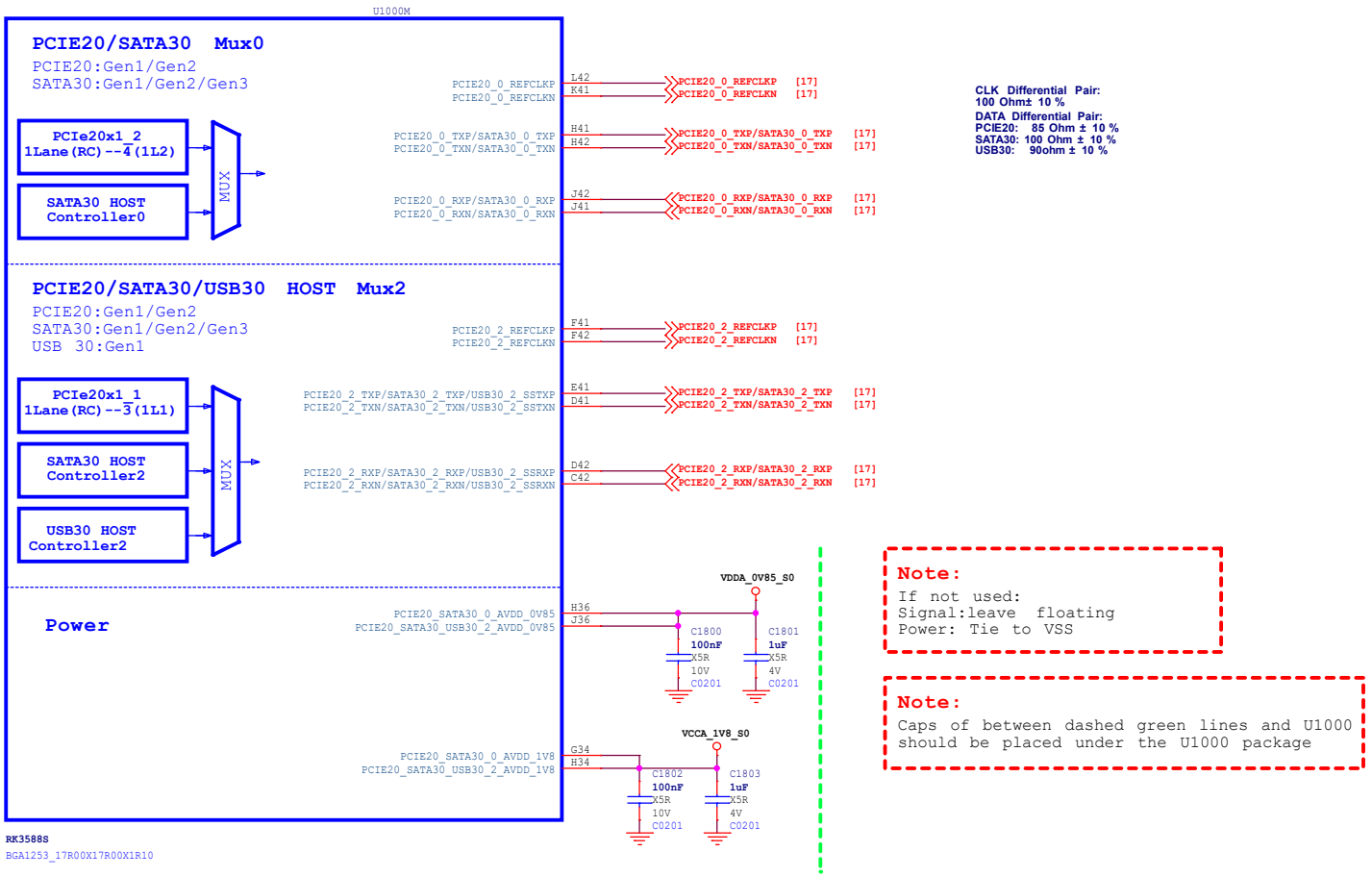


Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom https://armsom.org/					
Project:	ArmSOM-CM7S				
File:	RK3588S_HDMI/eDP Interface				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	10 of 18

RK3588S(PCIE20/SATA30/USB30)



Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

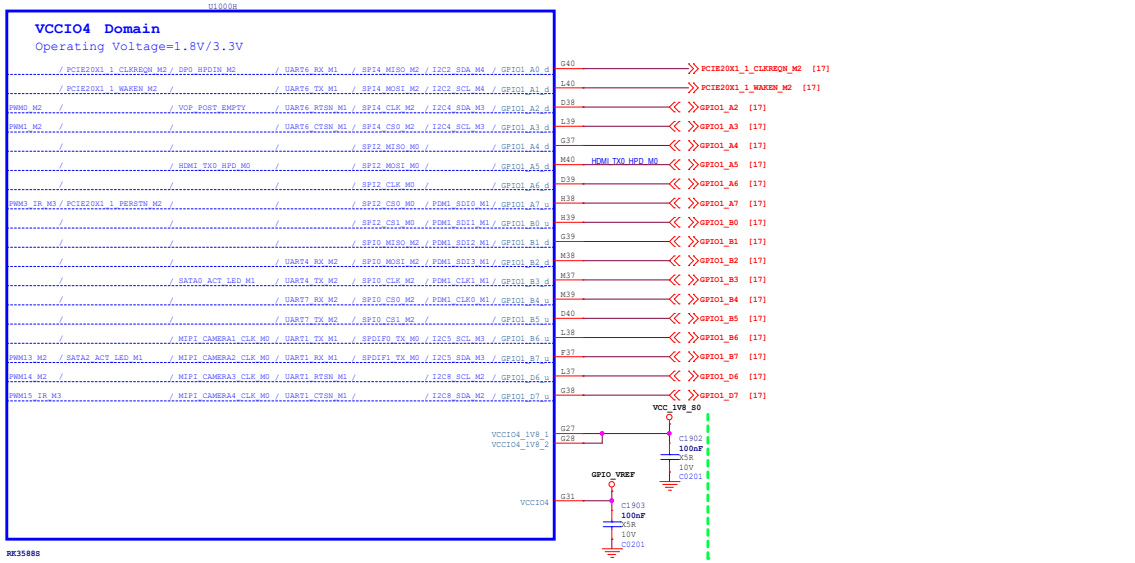
PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

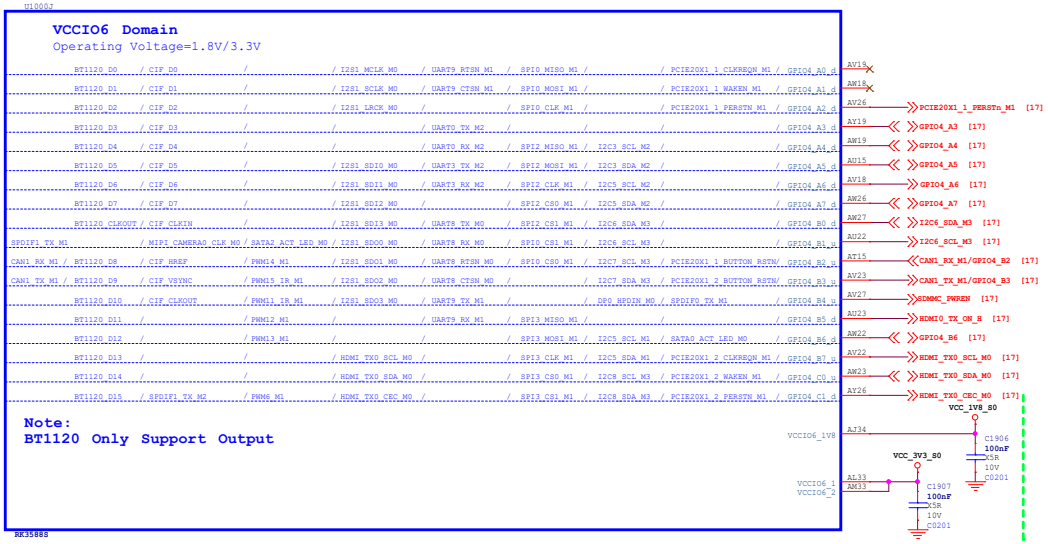
armsom https://armsom.org/

Project:	ArmSOM-CM7S				
File:	RK3588S PCIE2/SATA3/USB3 PHY				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	11 of 18

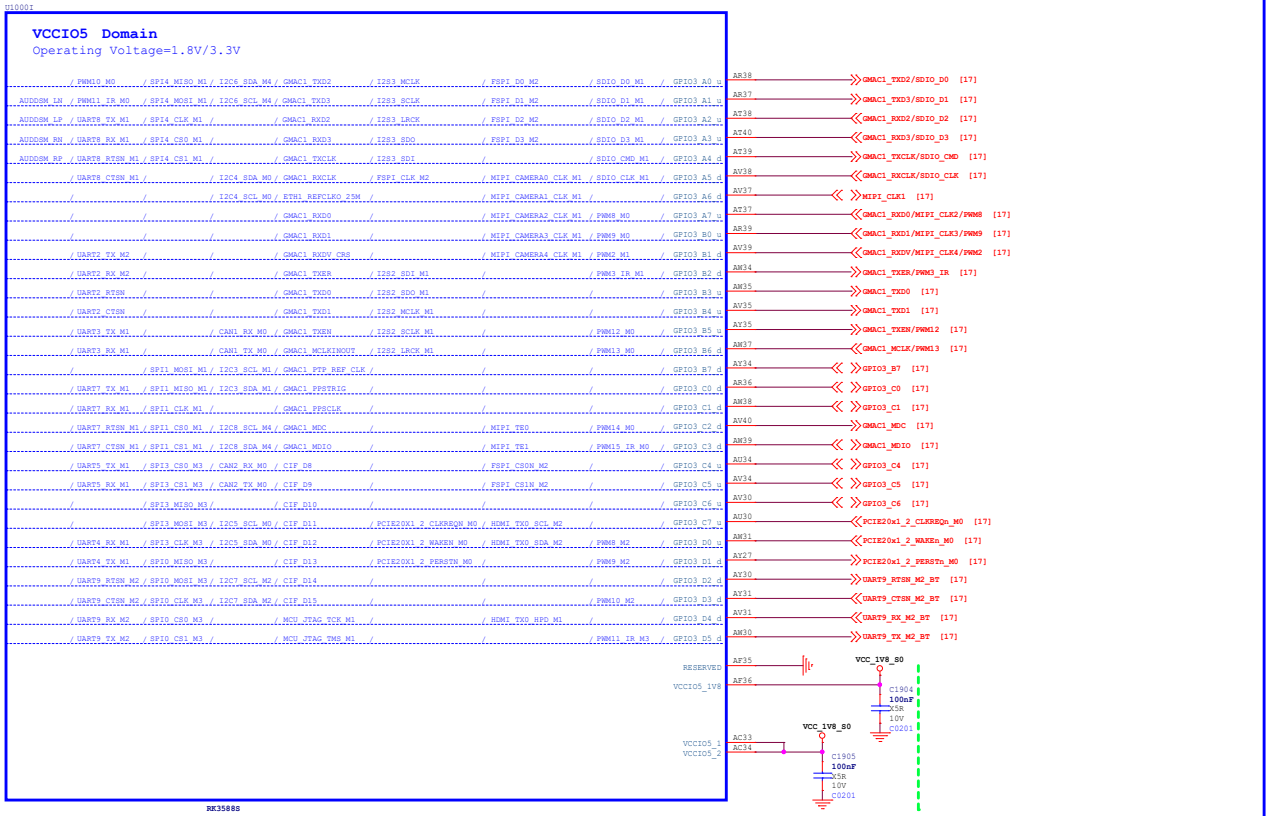
RK3588S(VCCIO4 Domain)

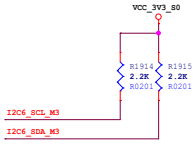


RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)





Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

armsom	https://armsom.org/				
Project:	ArmSOM-CM7S				
File:	RK3588S GPIO				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	12 of 18

PMIC1 RK806-1

SLEEP1_RESET1_DEVOFF1_VSEL1 [4]
PMIC_PWR_CTRL2 [4]
PMIC_INT_L [4]
PMIC_RESET_L [4,17]
PMIC_SPI_CLK [4]
PMIC_SPI_CS [4]
PMIC_SPI_MOSI [4]
PMIC_EXT_EN_OUT [14]

VCC_SYSIN
ED2200 AZ5825-01F ESD0402-6

IF TVS UNMOUNTED, ESD OR SURGE SHOULD BE DAMAGE THE PMIC!!!

This device must be mounted.Replacing TVS mode is not recommended, if must, please choose the same specifications
Operating Supply Vltage :5.5V(5.25-6V)
PeakPulse Current:>10A(tp=8/20uS)
Surge Clamping Voltage:<6.5V

DO NOT DELETE IT!

PMIC RK806-1 BUCK

U2200A

BUCK5 2.5A — BUCK1 6.5A
BUCK6 2.5A — BUCK2 5A
BUCK9 2.5A — BUCK3 5A
BUCK8 2.5A — BUCK4 5A
BUCK10 2.5A — BUCK7 2.5A

VDD_DDR_S0 0.80V Max:2.5A
Default:0.85V
Low frequency:
0.85V-->0.75V
0.675 0.85 0.935
PMIC_SW5 PMIC_VOUT5 PMIC_FB5 (FB=0.5V)
Feedback from RK3588S

VDD_GPU_S0 0.85V Max:6A
0.55 0.75 0.95
PMIC_SW1 PMIC_VOUT1 (FB=0.5V)
Feedback from RK3588S

VDD2_DDR_S3 1.10V 658mA Max:1.5A
1.045 1.1 1.155
PMIC_SW6 PMIC_VOUT6 PMIC_FB6 (FB=0.5V)

VDD_CPU_LIT_S0 0.95V Max:3A
0.55 0.75 0.95
PMIC_SW2 PMIC_VOUT2 (FB=0.5V)
Feedback from RK3588S

LPDDR4/4x=1.1V	120K
LPDDR5=1.05V	110K

VDDQ_DDR_S0 0.60V 232.60mA
0.57 0.6 0.63
0.475 0.5 0.525
PMIC_SW9 PMIC_VOUT9 PMIC_FB9 (FB=0.5V)

VDD_LOGIC_S0 0.75V Max:2A
0.675 0.75 0.825
PMIC_SW3 PMIC_VOUT3
Feedback from RK3588S

LPDDR4/4x=0.6V	20K	100K
LPDDR5=0.5V	0R	DNP

VCC_3V3_S3 Max:2.5A
PMIC_SW8 PMIC_VOUT8

VDD_VDENC_S0 0.775V
0.675 0.75 0.825
PMIC_SW4 PMIC_VOUT4
Feedback from RK3588

Default:1.8V Max:1A
PMIC_SW10 PMIC_VOUT10

VCC_2V0_PLDO_S3 2.0V 0.35A Max:0.5A
PMIC_SW7 PMIC_VOUT7

RK806-1
QFN68_7R00X7R00X0R80_T

PMIC RK806-1 Managerment

U2200C

VCCIO
VCCA

VCC_1V8_S3_PLDO6
VCC_SYSIN
VCC_1V8_S3

PMIC_SPI_CS
PMIC_SPI_MOSI
PMIC_SPI_CLK
PMIC_PWR_CTRL2
SLEEP1_RESET1_DEVOFF1_VSEL1
PMIC_EXT_EN_OUT
PMIC_INT_L
PMIC_RESET_L
PMIC_VDC
PWRON_L [17]

RK806-1
QFN68_7R00X7R00X0R80_T

RK3588S
nPOR
TSADC_SHUT
RK806-1
RESETB
Reset Key

Note:
- Reset Key Control Path
- TSADC_SHUT Control Path
- RK806-1 Control Path

PMIC RK806-1 LDO

U2200B

PLDO
NLDO

VCCA_1V8_S0	200mA	PLDO1	Default:1.8V
VCC_1V8_S0	150mA	PLDO2	Default:1.8V
VDDA_1V2_S0	2mA	PLDO3	Default:1.2V
VCCA_3V3_S0	200mA	PLDO4	Default:3.3V
VCCIO_SD_S0	1mA	PLDO5	Default:3.3V
VDD_0V75_S3	10mA	NLDO1	Default:0.75V
VDDA_DDR_PLL_S0	126mA	NLDO2	Default:0.85V; Low frequency:0.85V-->0.75V
VDDA_0V75_S0	150mA	NLDO3	Default:0.75V
VDDA_0V85_S0	330mA	NLDO4	Default:0.85V
HDMI_VDDA0V85_S0		NLDO5	Actual Setting 0.8375V

VCC_2V0_PLDO_S3
VCC_SYSIN
VCC_1V1_NLDO_S3 600mA
VCC_1V1_NLDO_S3

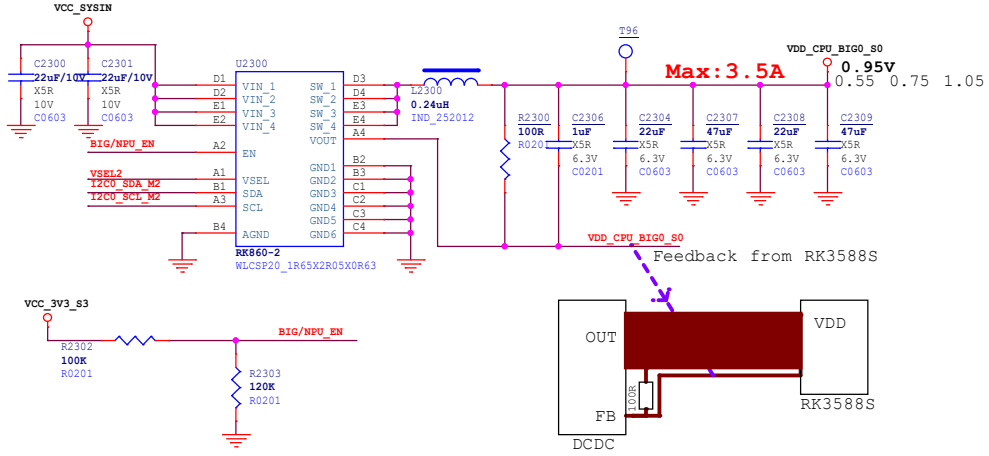
2.70 3.30 3.60
1.65 1.80 1.95

RK806-1
QFN68_7R00X7R00X0R80_T

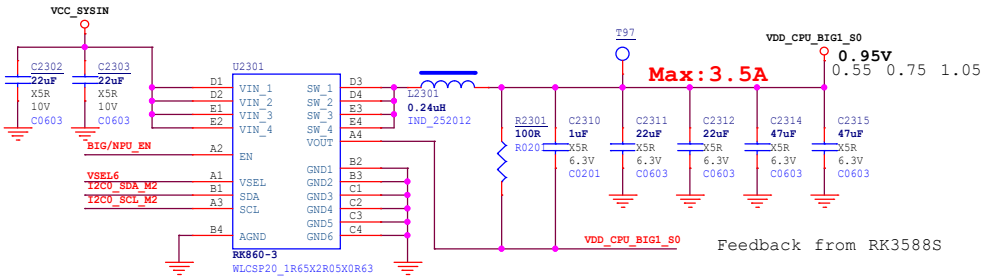
armsom https://armsom.org/

Project:	ArmSOM-CM7S				
File:	Power-PMIC_RK806-1				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	13 of 18

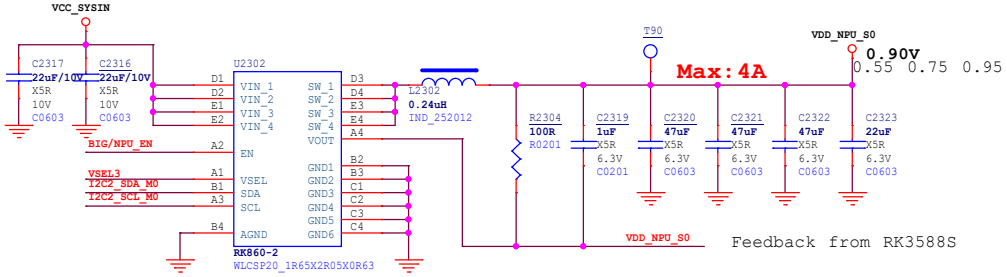
VDD_CPU_BIG0



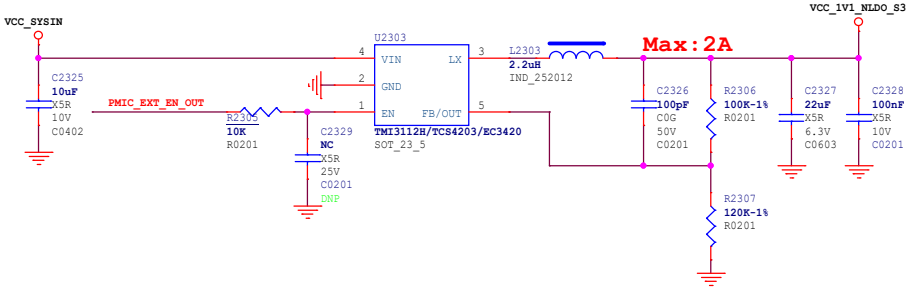
VDD_CPU_BIG1



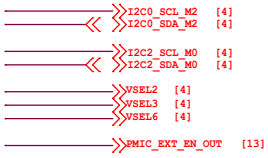
VDD_NPU

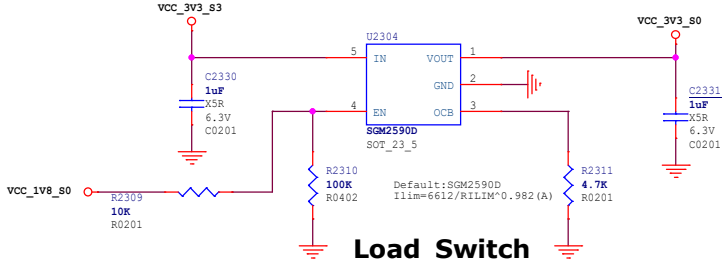


VCC_1V1_NLDO



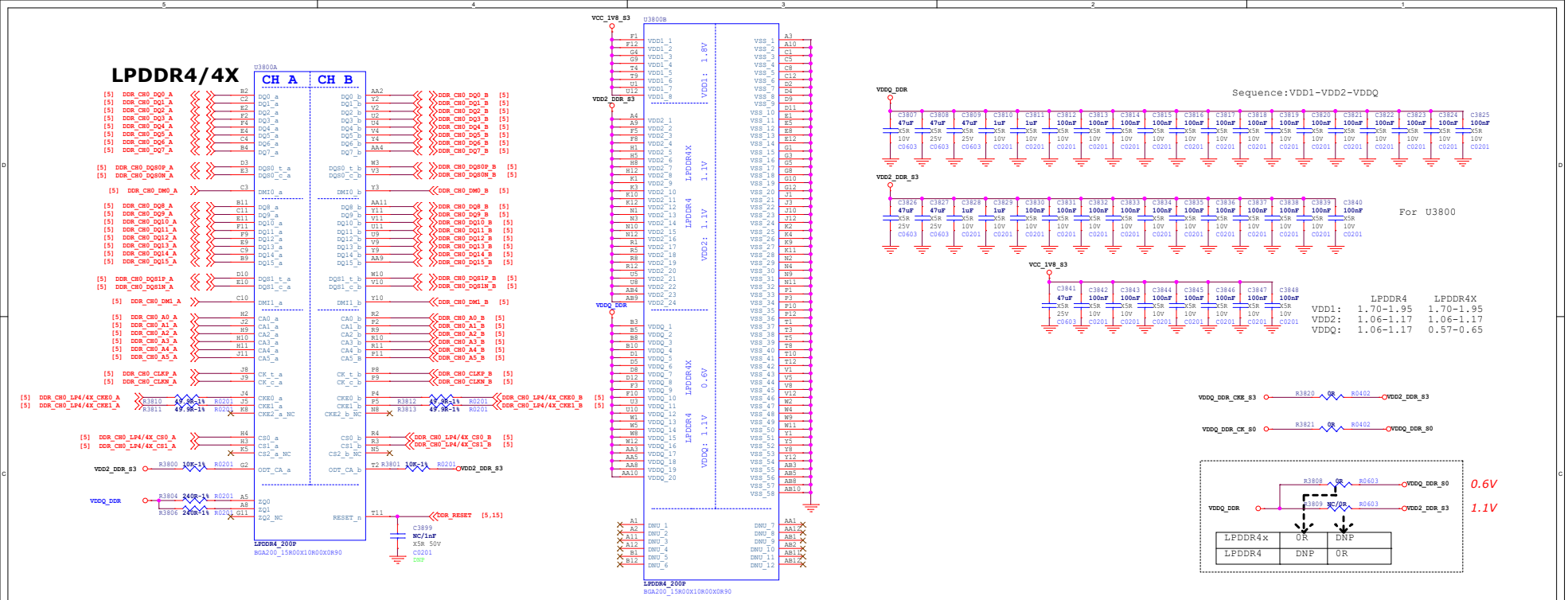
VCC_3V3_S0



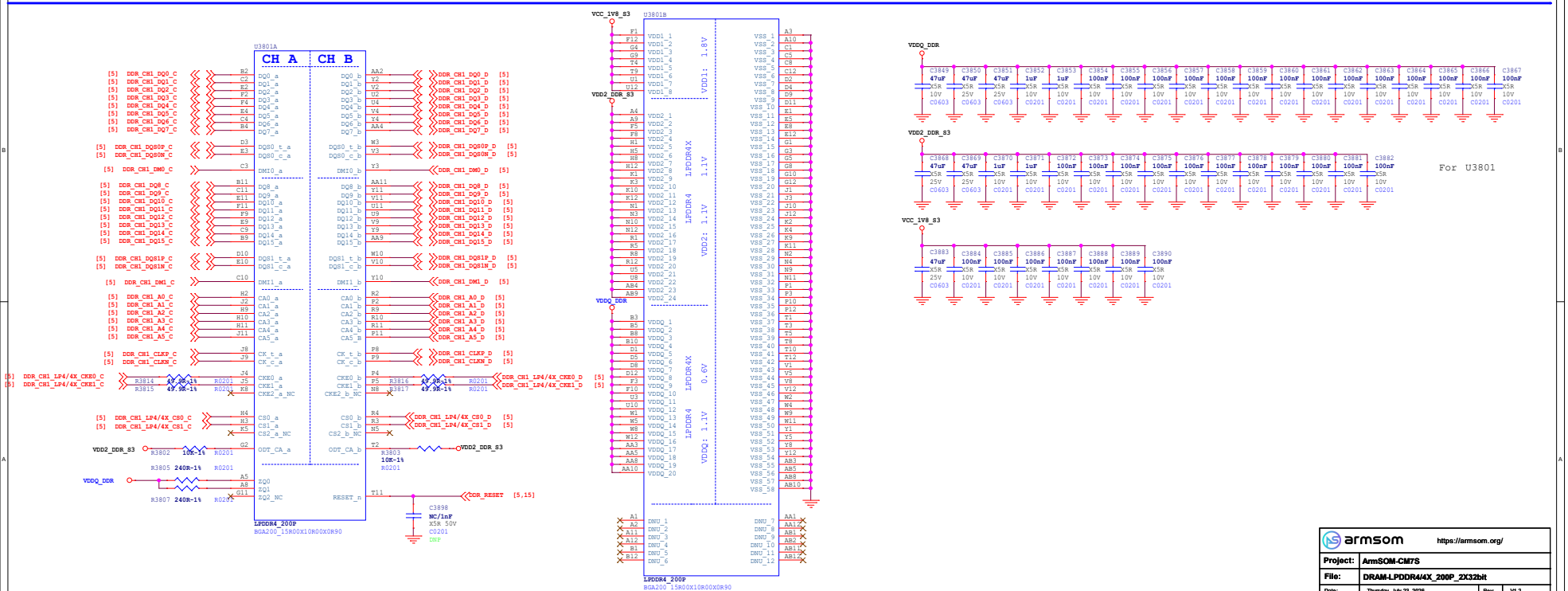


armsom	https://armsom.org/			
Project:	ArmSOM-CM7S			
File:	Power_Ext Discrete			
Date:	Thursday, July 23, 2026		Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet: 14 of 18

LPDDR4/4X



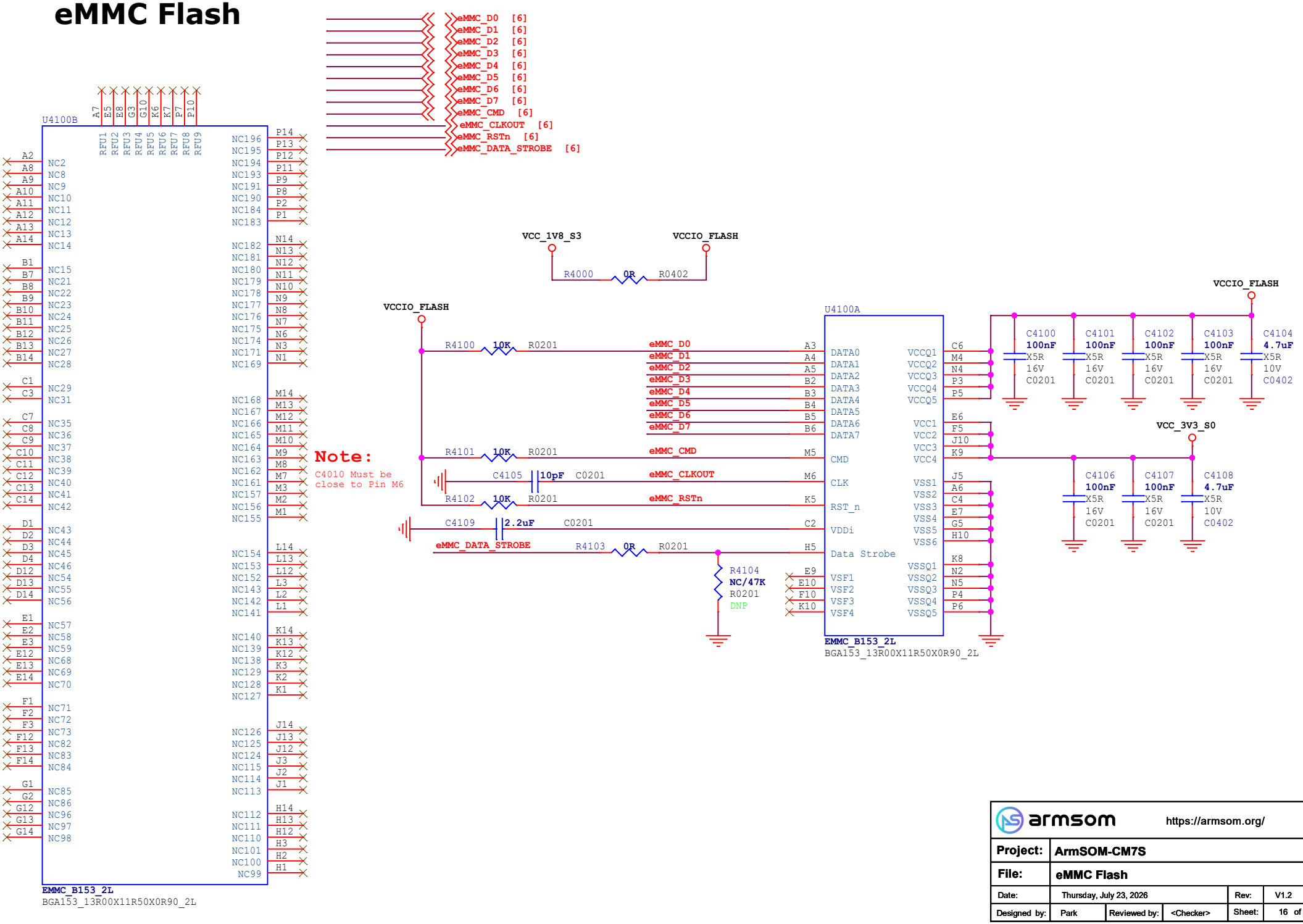
H9HCNNNCPMMLXR-NEE 200FBGA LPDDR4X 4266Mbps 4GB



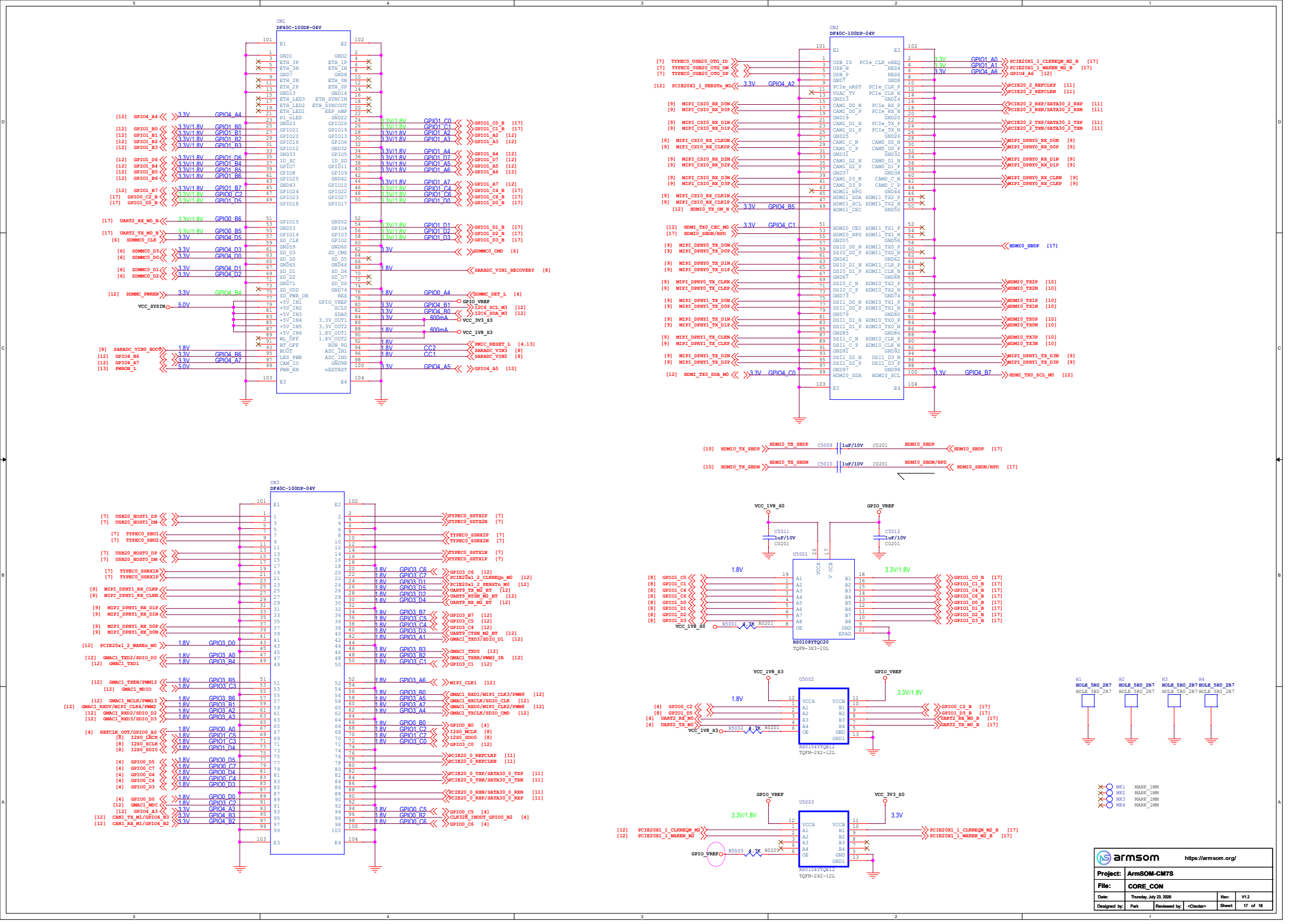
H9HCNNNCPMMLXR-NEE 200FBGA LPDDR4X 4266Mbps 4GB

armsom	https://armsom.org/		
Project:	ArmSOM-CM7S		
File:	DRAM-LPDDR4/4X_200P_2X32bit		
Date:	Thursday, July 23, 2026	Rev:	V1.2
Designed by: Park	Reviewed by: <Checker>	Sheet:	15 of 18

eMMC Flash



armsom	https://armsom.org/				
Project:	ArmSOM-CM7S				
File:	eMMC Flash				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	16 of 18


CN1
DF40C-100DP-04V
CN2
DF40C-100DP-04V
CN3
DF40C-100DP-04V
U5001
RS0108YTQC20
TQFN-3X3-20L
U5002
RS0104YTQB12
TQFN-2X2-12L
U5003
RS0104YTQB12
TQFN-2X2-12L
armsom
https://armsom.org/
Project: ArmSOM-CM7S
File: CORE_CON
Date: Thursday, July 23, 2026
Rev: V1.2
Designed by: Park
Reviewed by: <Checker>
Sheet: 17 of 18

Revision History

Version	Date	By	Change Dsecription	Approved
V1.0	2025-11-07	Park	Frist release;	
V1.1	2026-07-07	Park	add logo and change project name;	
V1.2	2026-07-23	Park	U5003 pin6=VCC_1V8_S0 change to GPIO-VREF;	

armsom	https://armsom.org/				
Project:	ArmSOM-CM7S				
File:	Revision History				
Date:	Thursday, July 23, 2026			Rev:	V1.2
Designed by:	Park	Reviewed by:	<Checker>	Sheet:	18 of 18