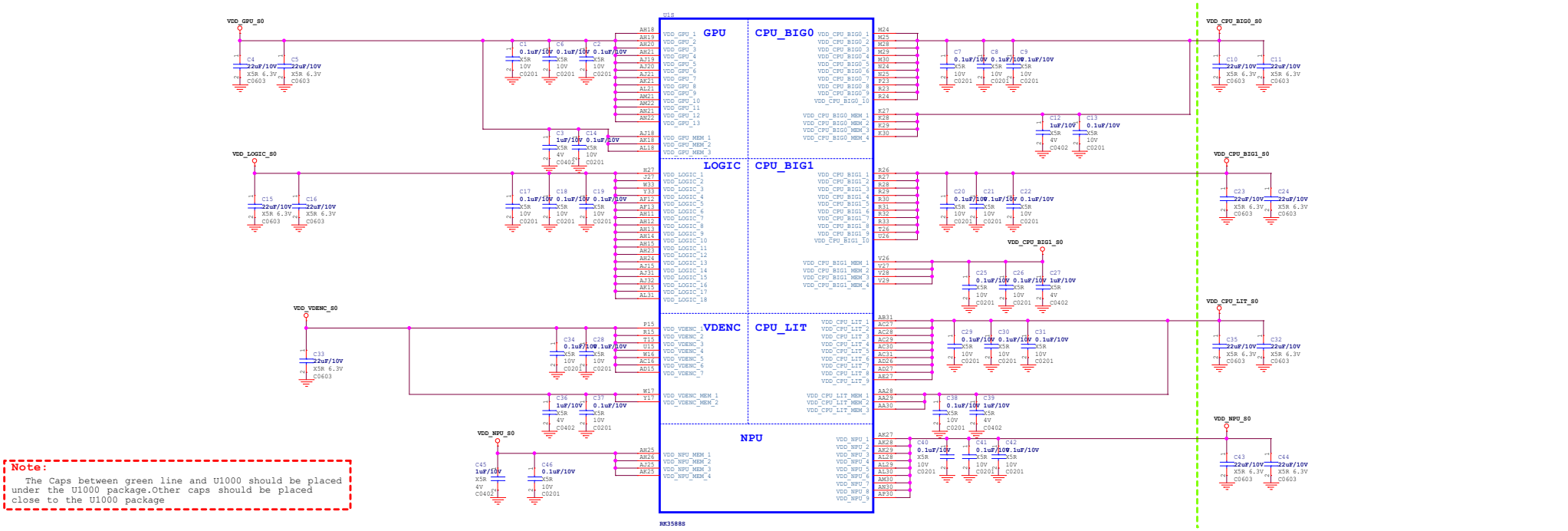
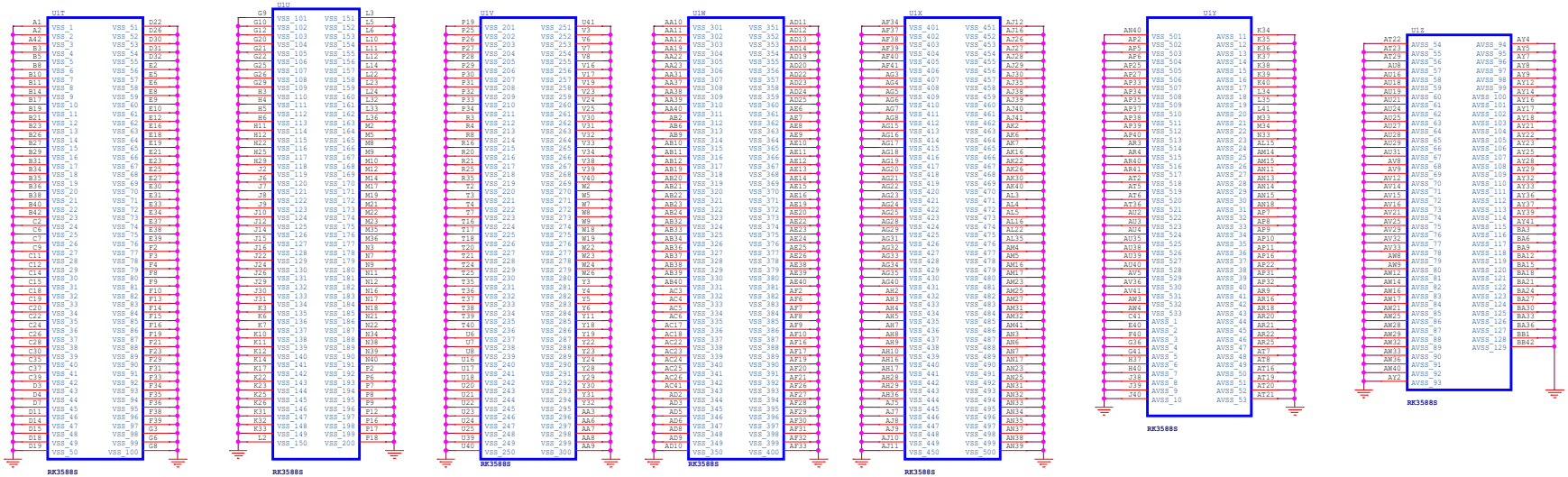
RK3588S(Power&Gnd)



Note:

The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package



Rockchip Confidential

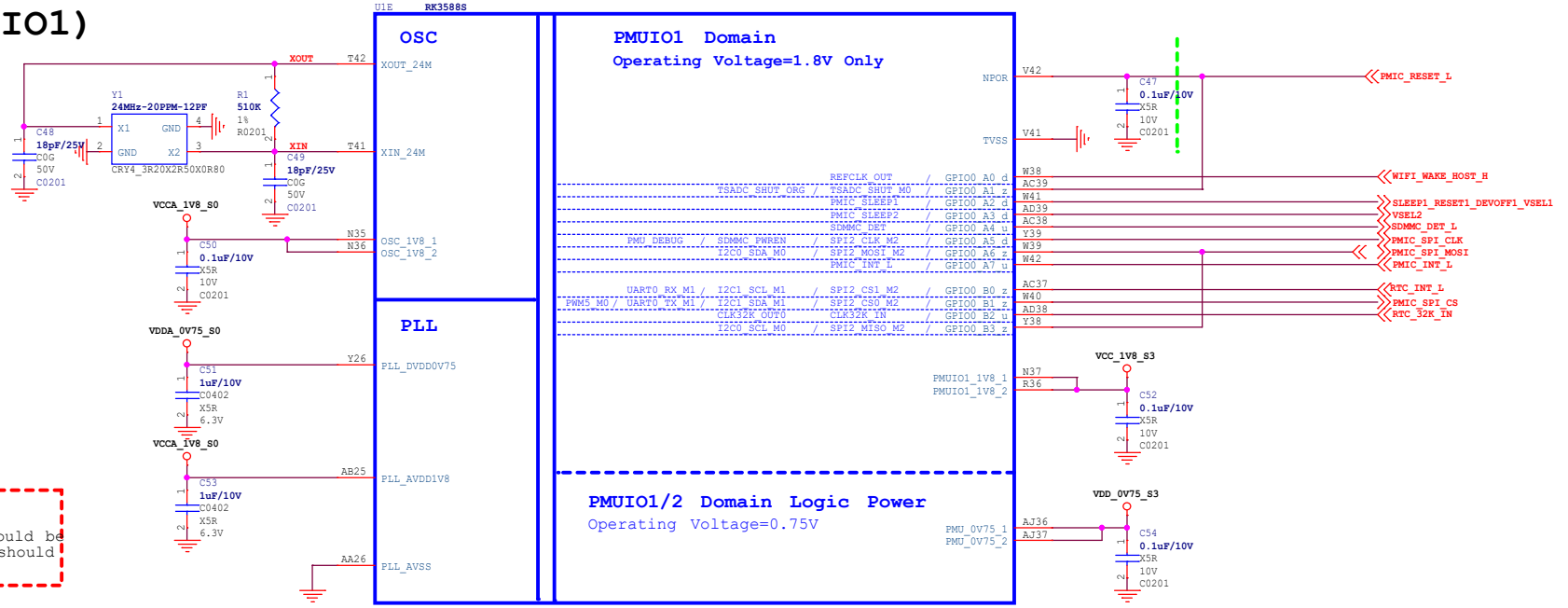
Rockchip	Rockchip Electronics Co., Ltd		
Project:	ArmSoM-Sige7s		
File:	<Page name>		
Date:	Monday, April 13, 2026	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet: 1 of 23

RK3588S(OSC/PLL/PMUIO1)

Note:
Adjusted the load capacitance according to the crystal specification

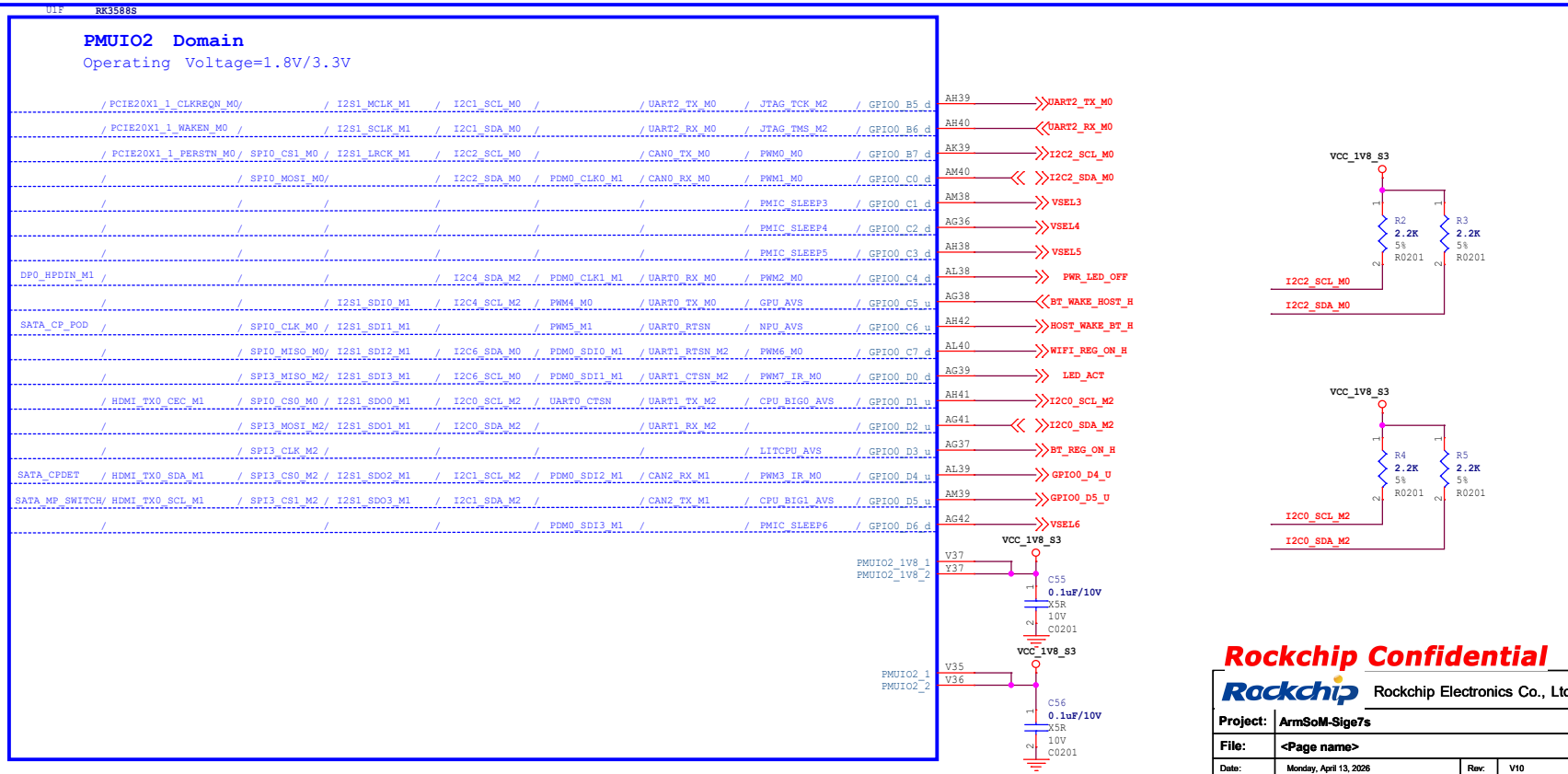
The CL is the load capacitance of the crystal that is recommended by the crystal vendors to obtain target clock frequency.

CL={CL1*CL2/(CL1+CL2))}+PCB strays
Total CL<=12pF



Note:
The Caps between green line and U1000 should be placed under the U1000 package.Other caps should be placed close to the U1000 package

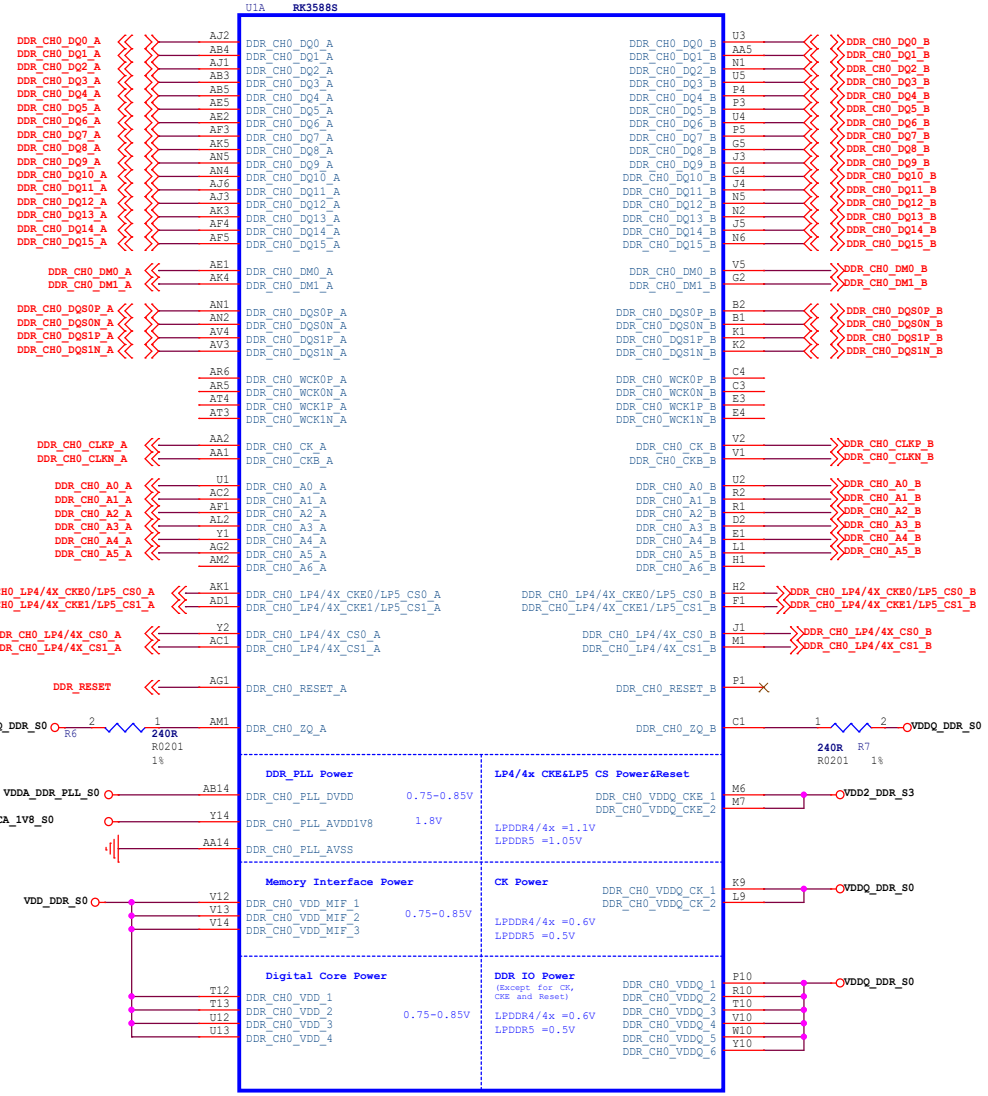
RK3588S(PMUIO2)

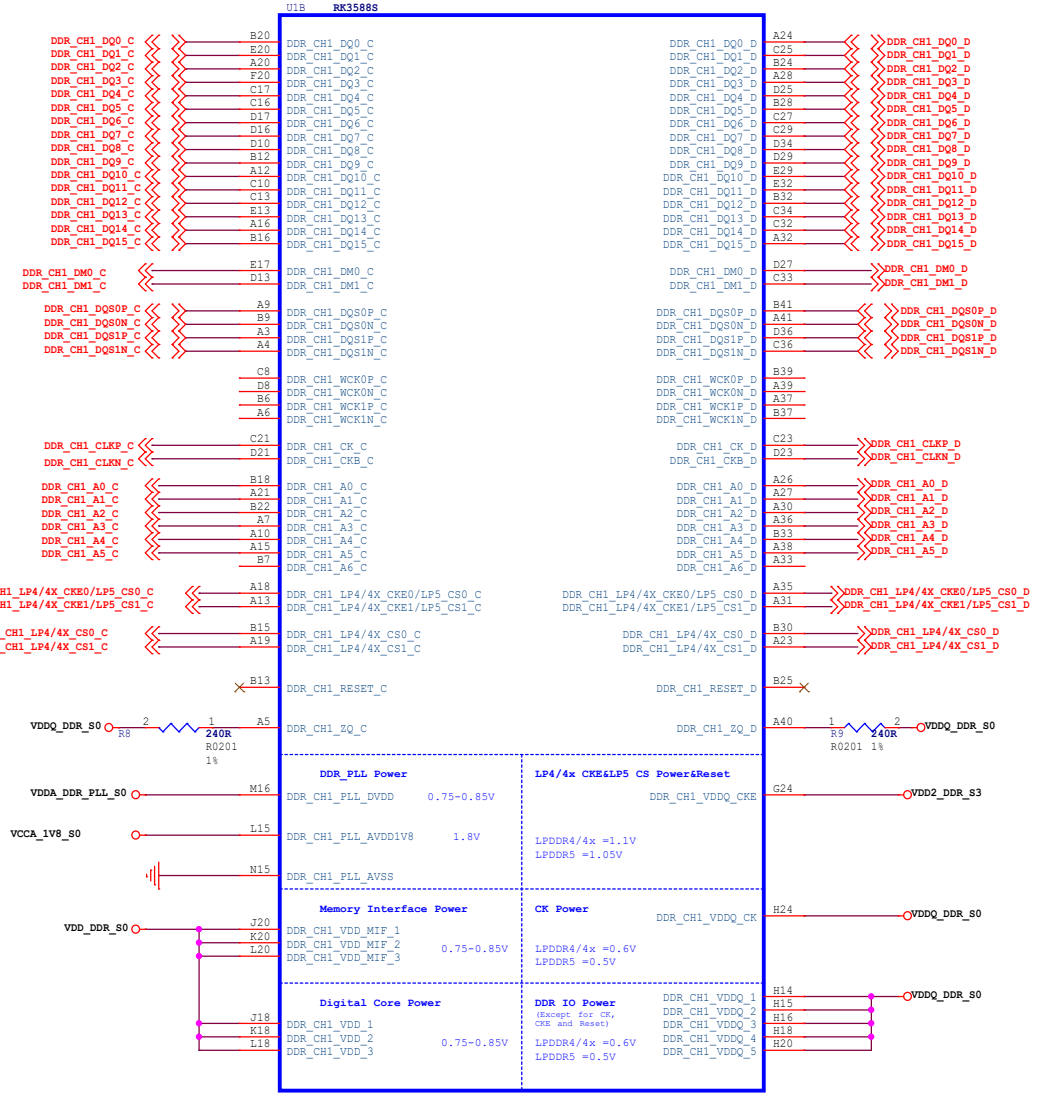


Rockchip Confidential

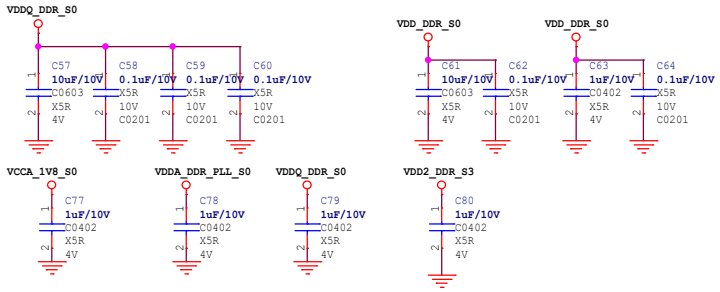
Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	2 of 23

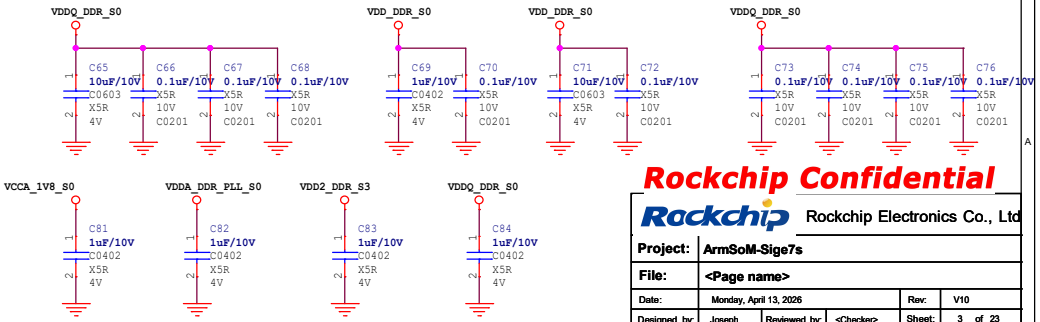
RK3588S(DDR PHY)





DDR FILTER

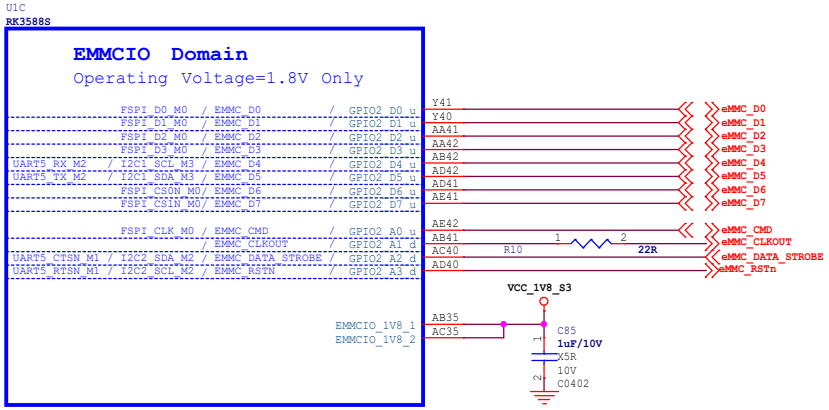




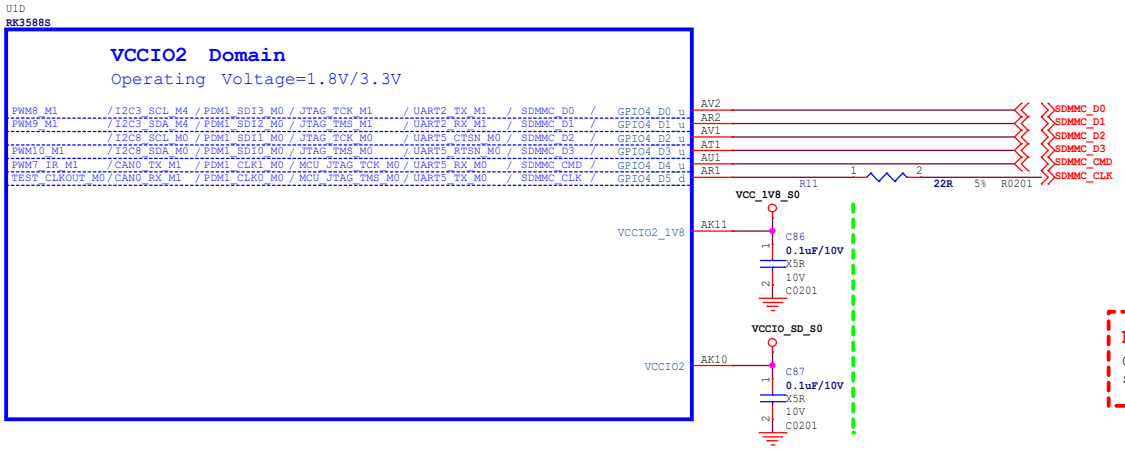
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	3 of 23

RK3588S(EMMCIO Domain)



RK3588S(VCCIO2 Domain)

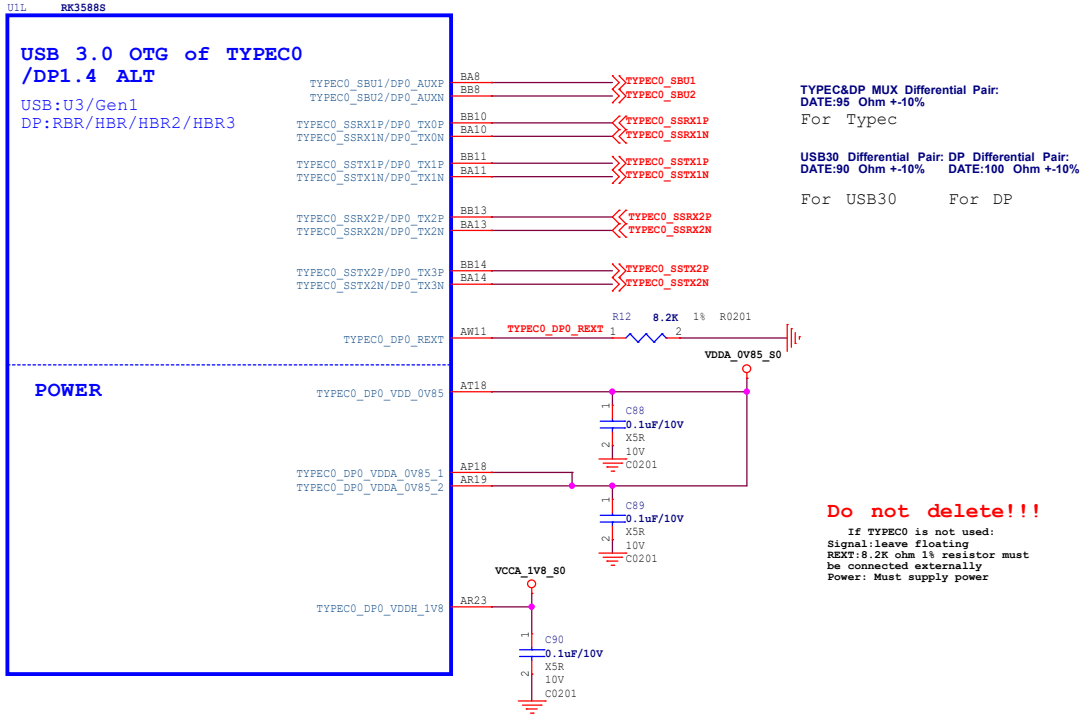


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	4 of 23

RK3588S(USB3.0/DP1.4)

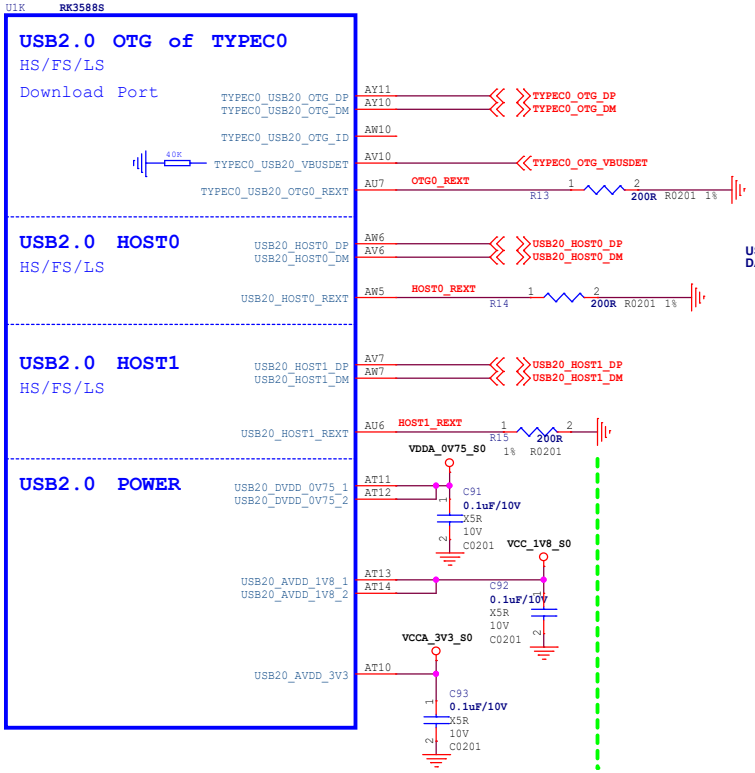


USB30/DP1.4 Alt Mode Configuration

Option1	*DP x4Lane*	*DP_TX_Lane0-3*
Option2	*TYPEC x4Lane*	*SSTX 1P/1N SSTX 2P/2N SSRX 1P/1N SSRX 2P/2N*
Option3	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 1P/1N SSRX 1P/1N DP:Lane2 Lane3*
Option4	*USB30X2Lane+DPX2Lane*	*USB30:SSTX 2P/2N SSRX 2P/2N DP:Lane0 Lane1*

DP Lane
Swap Off:
Lane0/1/2/3_TXdata mapping to Lane0/1/2/3_TXDP/N
Swap On:
Lane0/1/2/3_TXdata mapping to Lane2/3/0/1_TXDP/N

RK3588S(USB2.0)



Note:
The USB20_VBUSDET pin internal has a pull-down resistance(40K ohm) to ground,The resistance creates a voltage with the external series 24K ohm resistor.The VBUSDETpin voltage range <=3.3V.

Note:
TYPEC0_USB20_OTG:

DP/DM:Must used for download
ID:According to demand,if not used,Leave floating
VBUSDET:Must provide
REXT:200ohm 1% resistor must be connected externally
Power: Must supply power

USB20_HOST0/USB20_HOST1:

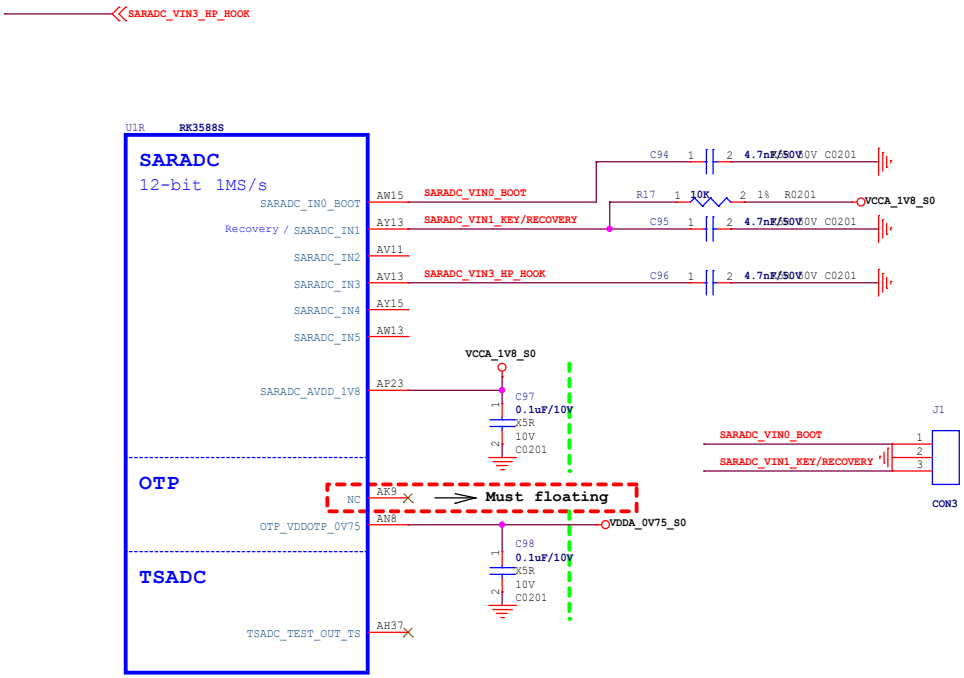
If not used:
DP/DM:Leave floating
REXT:Leave floating

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

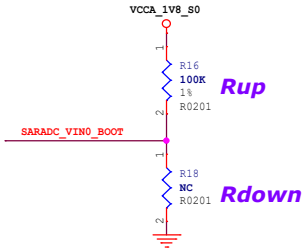
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	5 of 23

RK3588S(SARADC/OTP/TSADC)

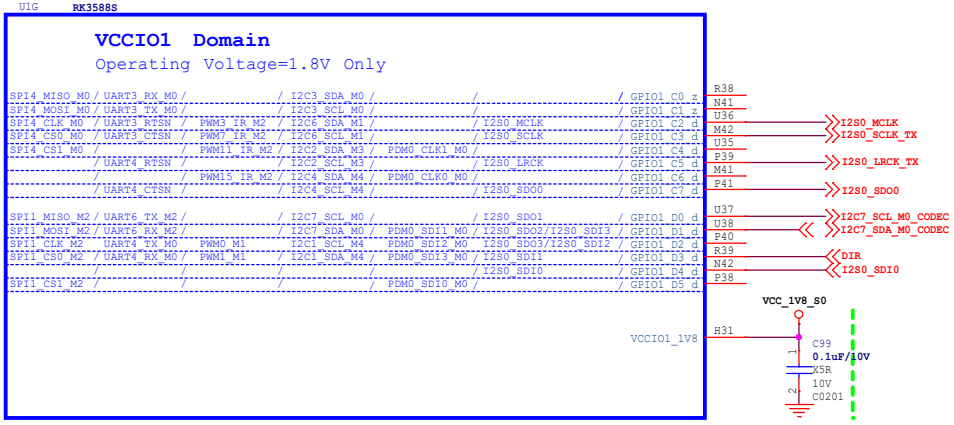


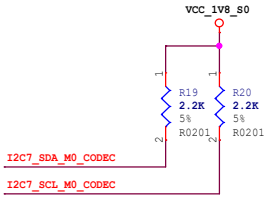
BOOT MODE CONFIG



Item	Rup	Rdown	ADC	BOOT MODE(saradc_in5)
LEVEL1	DNP	100K	0	USB (Maskrom mode)
LEVEL2	100K	20K	682	SD Card-USB
LEVEL3	100K	51K	1365	EMMC-USB
LEVEL4	100K	100K	2047	FSPI M0-USB
LEVEL5	100K	200K	2730	FSPI M1-USB
LEVEL6	100K	499K	3412	FSPI M2-USB
LEVEL7	100K	DNP	4095	FSPI_M2-FSPI_M0-EMMC -SD Card-USB

RK3588S(VCCIO1 Domain)



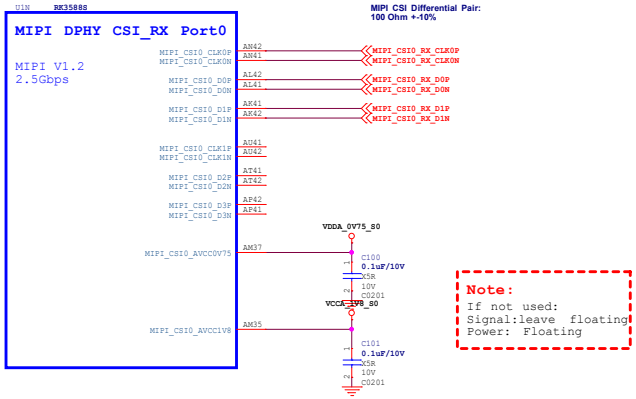


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	6 of 23

RK3588S(MIPI_DPHY CSI0 RX)



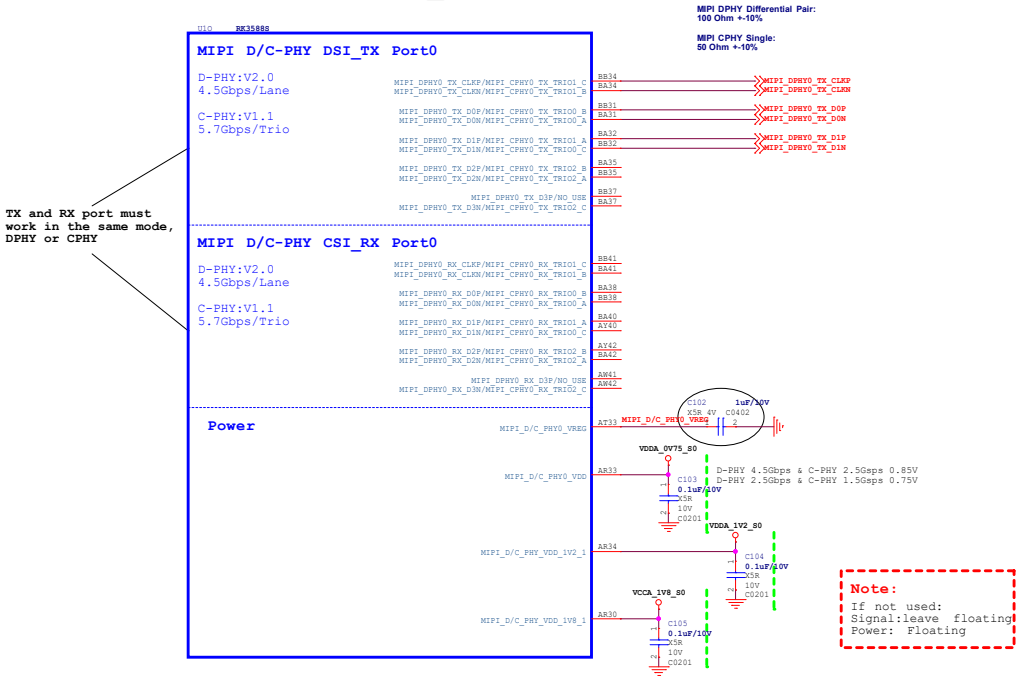
Note:
If not used:
Signal:leave floating
Power: Floating

Option1	*Sensor1 x4Lane*	*MIPI_CSI_RX_D0-3* *MIPI_CSI_RX_CLK0*
Option2	*Sensor1 x2Lane* *+* *Sensor2 x2Lane*	*MIPI_CSI_RX_D0-1* *MIPI_CSI_RX_CLK0* *MIPI_CSI_RX_D2-3* *MIPI_CSI_RX_CLK1*

Note:
When in single clock lane mode, CLK0P/0N is the clock lane from Data lane0 to Data lane3,but clock lane1 is invalid; In dual clock lanes mode,CLK0P/0N is the clock lane of Data lane0 and Data lane1,while CLK1P/1N is the clock lane of Data lane2 and Data lane3.

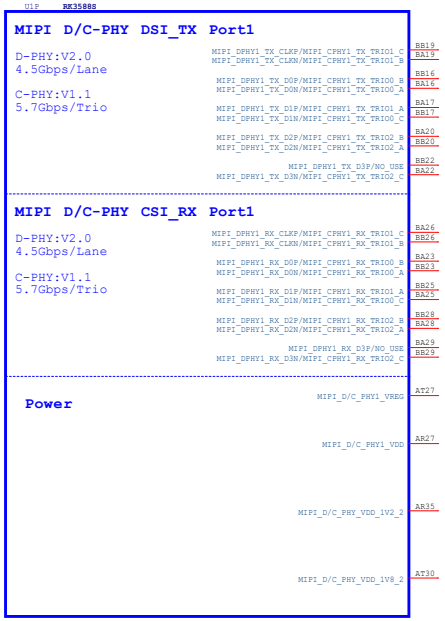
Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3588S(MIPI_D/C PHY0)



Note:
If not used:
Signal:leave floating
Power: Floating

RK3588S(MIPI_D/C PHY1)



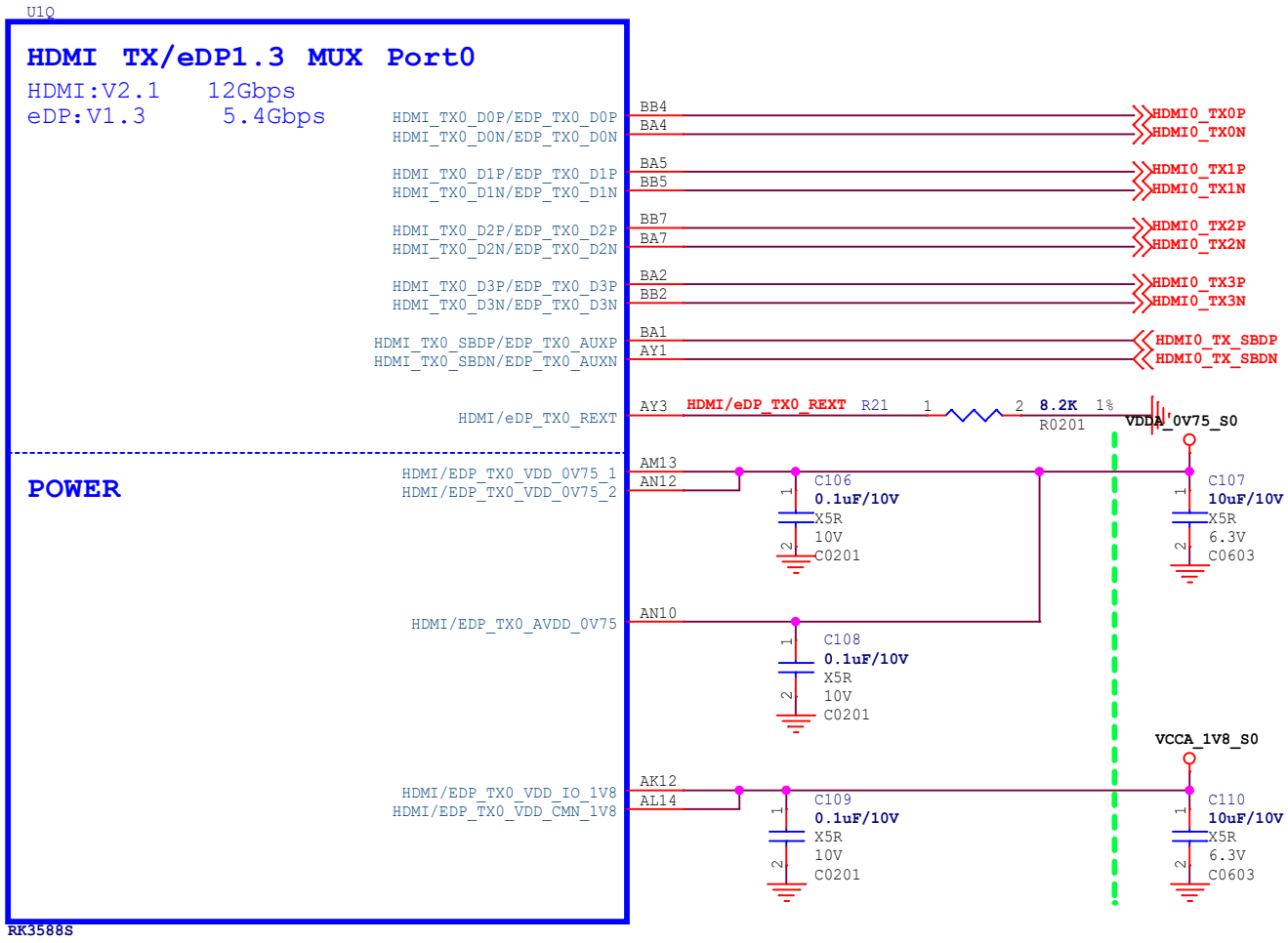
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd
Project:	ArmSoM-Sige7s
File:	<Page name>
Date:	Monday, April 13, 2026
Rev:	V10
Designed by:	Joseph
Reviewed by:	<Checker>
Sheet:	7 of 23

RK3588S(HDMI2.1 TX/eDP1.3 TX)

Note:
The HDMI2.1 trace length is less than 100mm.
The HDMI2.1 differential trace impedance is 100 OHM.

HDMI TX
100 Ohm ± 10 %



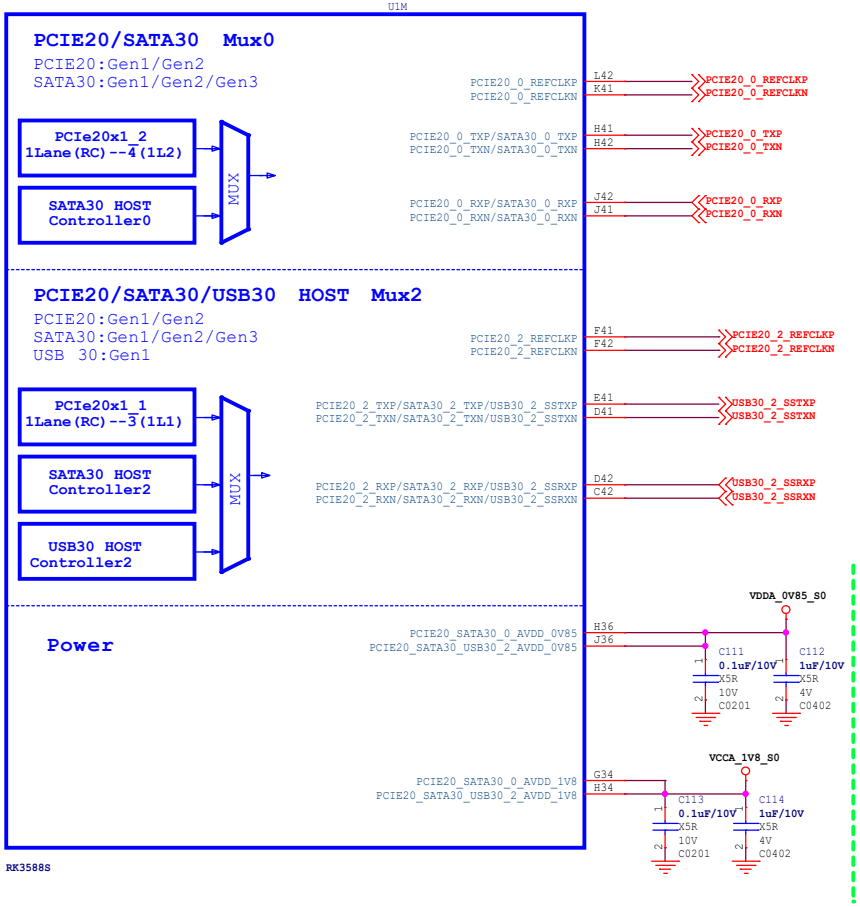
Note:
If not used:
Signal:leave floating
Power: Floating or tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	8 of 23

RK3588S(PCIE20/SATA30/USB30)



CLK Differential Pair:
100 Ohm± 10 %

DATA Differential Pair:
PCIE20: 85 Ohm ± 10 %
SATA30: 100 Ohm ± 10 %
USB30: 90ohm ± 10 %

Note:
If not used:
Signal:leave floating
Power: Tie to VSS

Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

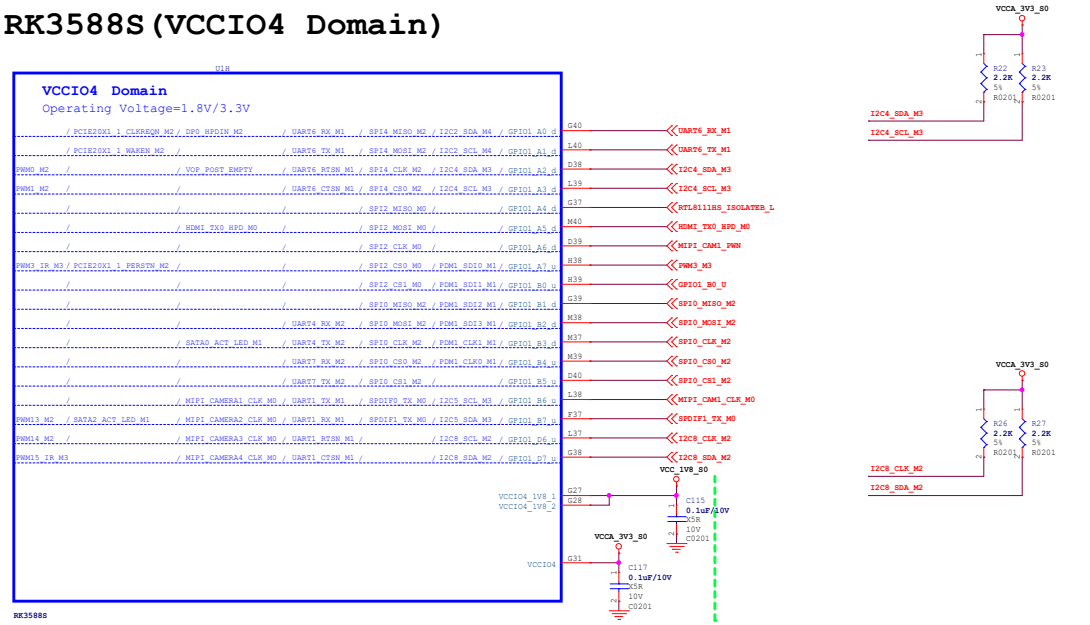
PCIe2.0 PHY

Controller Name	Data & Clk Lane Configure		Control GPIO
	CLK LANE	DATA LANE	
PCIE20X1_1 RC	PCIE20_2_REFCLKP PCIE20_2_REFCLKN	PCIE20_2_TX PCIE20_2_RX	PCIE20X1_1_CLKREQ_M* PCIE20X1_1_WAKEN_M* PCIE20X1_1_PERSTN_M* PCIE20X1_1_BUTTON_RSTN
PCIE20X1_2 RC	PCIE20_0_REFCLKP PCIE20_0_REFCLKN	PCIE20_0_TX PCIE20_0_RX	PCIE20X1_2_CLKREQ_M* PCIE20X1_2_WAKEN_M* PCIE20X1_2_PERSTN_M* PCIE20X1_2_BUTTON_RSTN

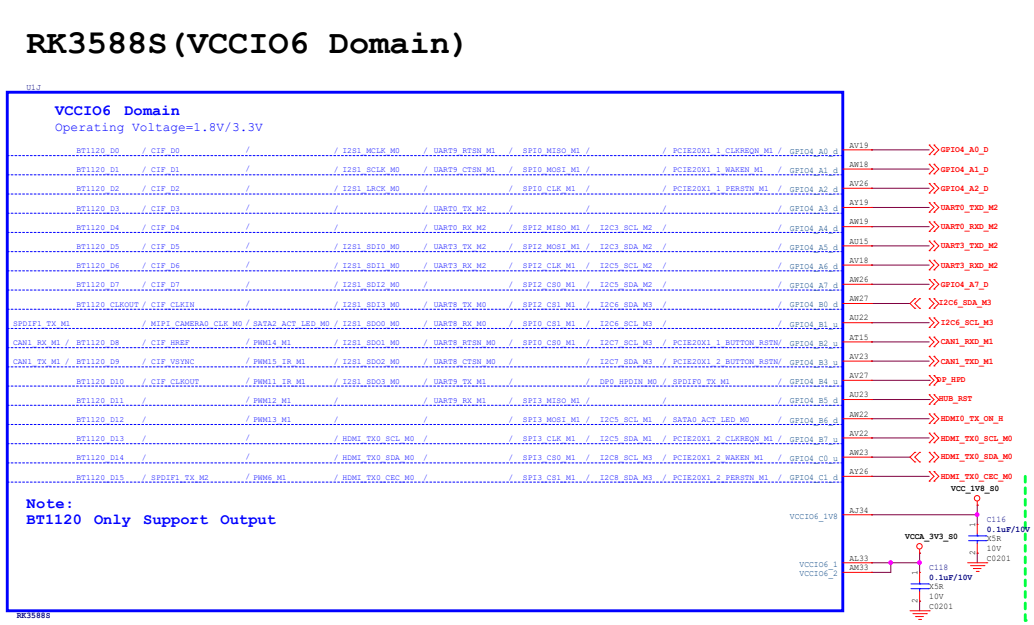
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	9 of 23

RK3588S(VCCIO4 Domain)

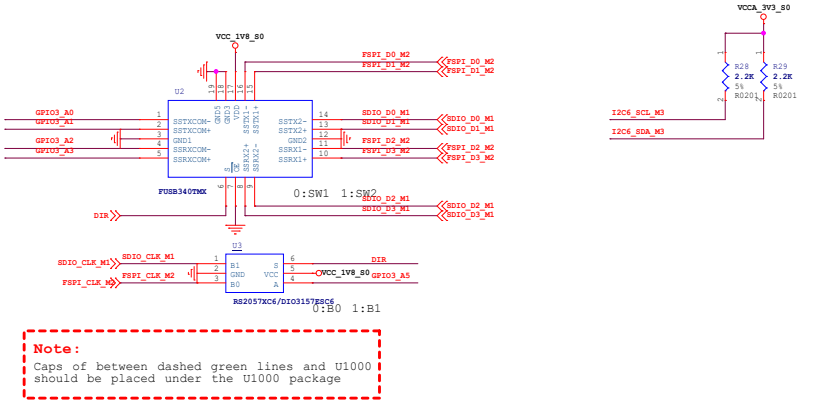


RK3588S(VCCIO6 Domain)



RK3588S(VCCIO5 Domain)



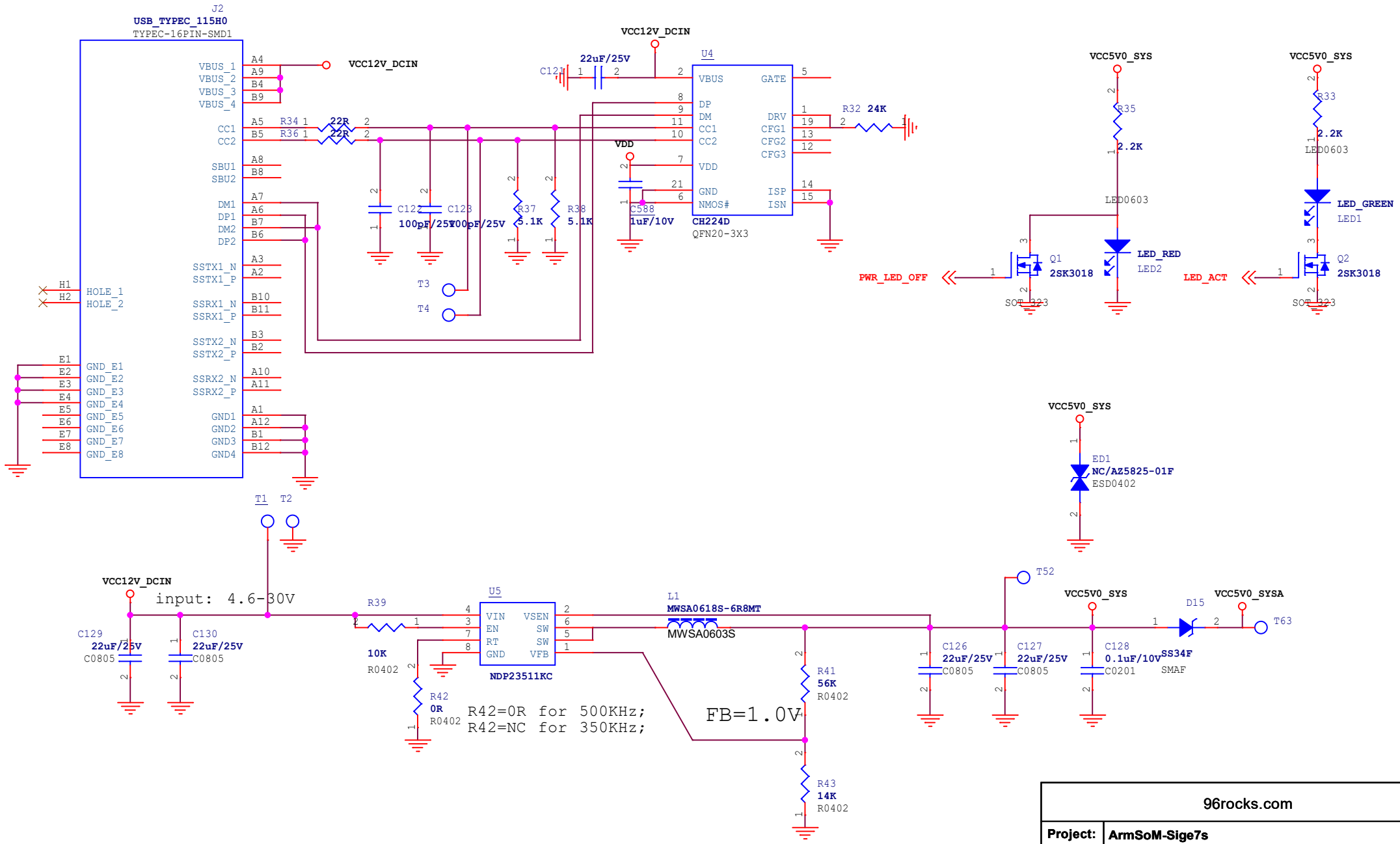


Note:
Caps of between dashed green lines and U1000 should be placed under the U1000 package

Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	ArmSoM-Sige7s		
File:	<Page name>		
Date:	Monday, April 13, 2026	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet: 10 of 23

DC IN&SYSTEM Power

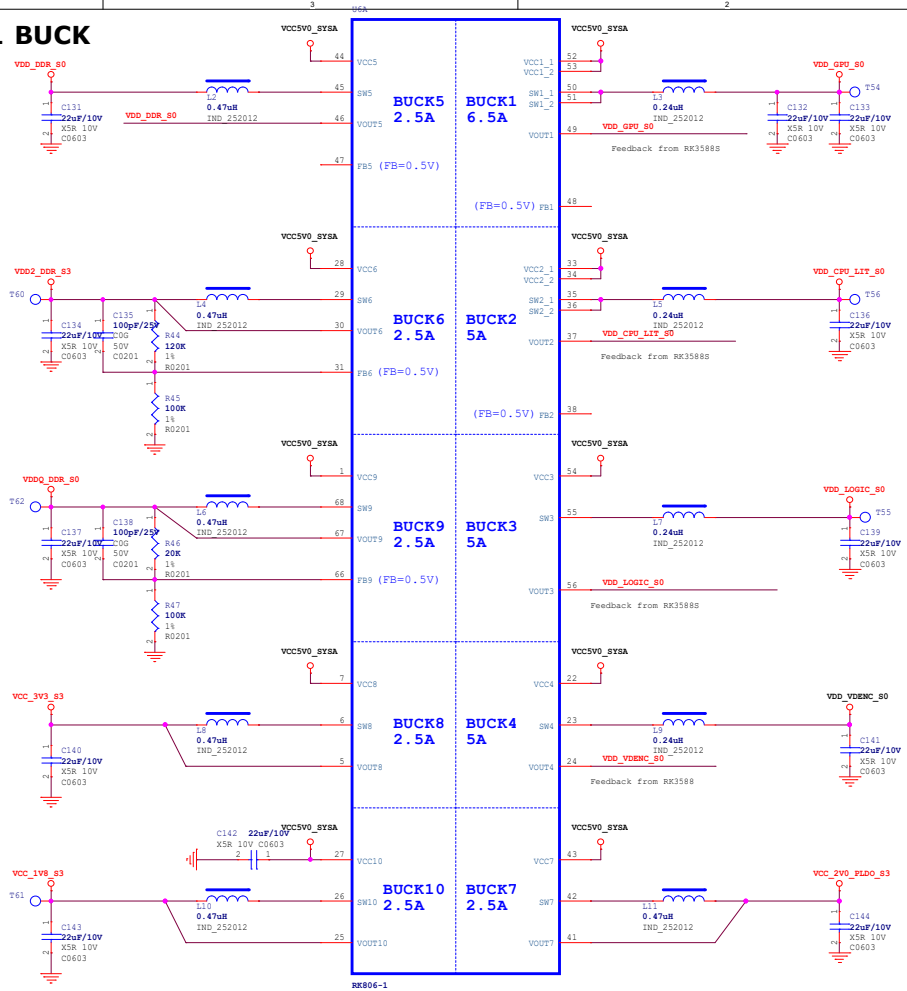


96rocks.com			
Project:	ArmSoM-Sige7s		
File:	<Page name>		
Date:	Monday, April 13, 2026	Rev:	V1.0
Designed by:	<designer>	Sheet:	11 of 23

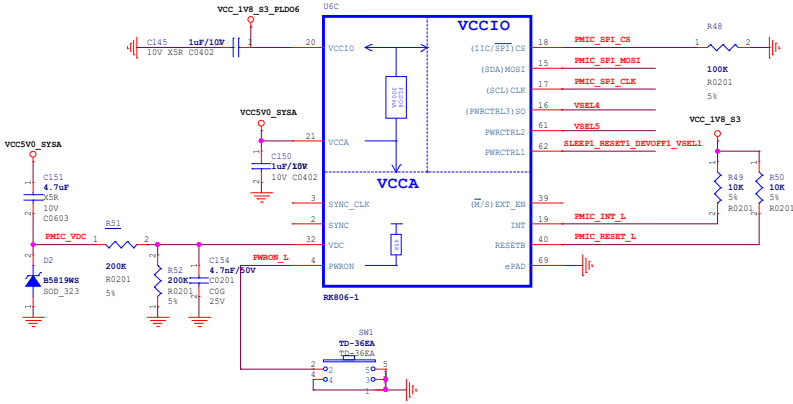
PMIC1 RK806-1



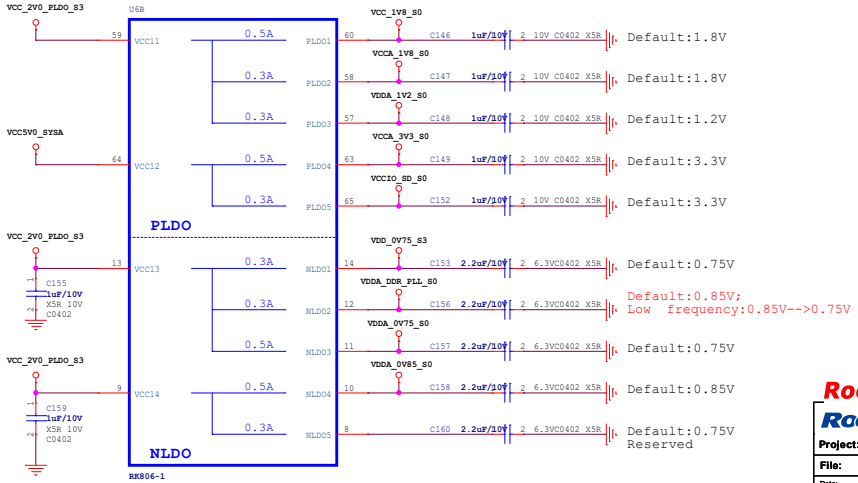
PMIC RK806-1 BUCK



PMIC RK806-1 Managerment



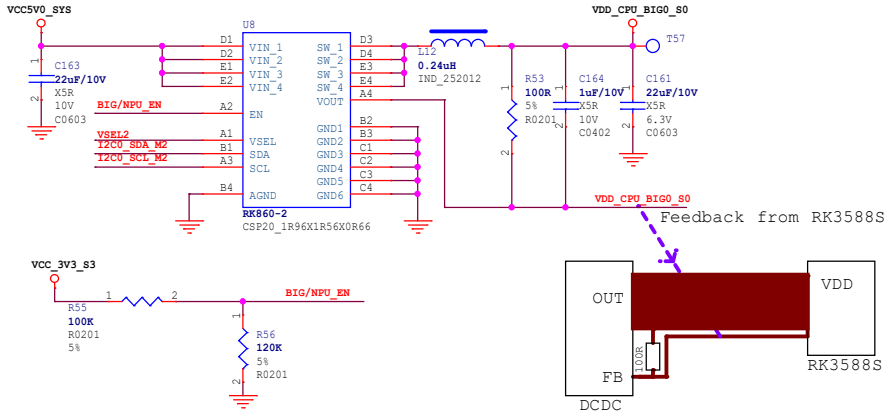
PMIC RK806-1 LDO



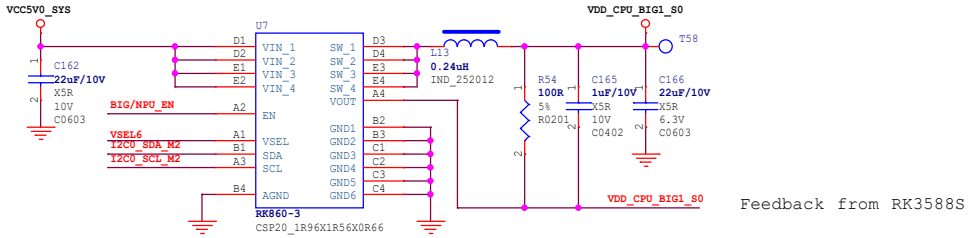
Rockchip Confidential

Rockchip Electronics Co., Ltd			
Project:	ArmSoM-Sige7s		
File:	<Page name>		
Date:	Monday, April 13, 2026	Rev:	V10
Designed by: Joseph	Reviewed by: <Checker>	Sheet:	12 of 23

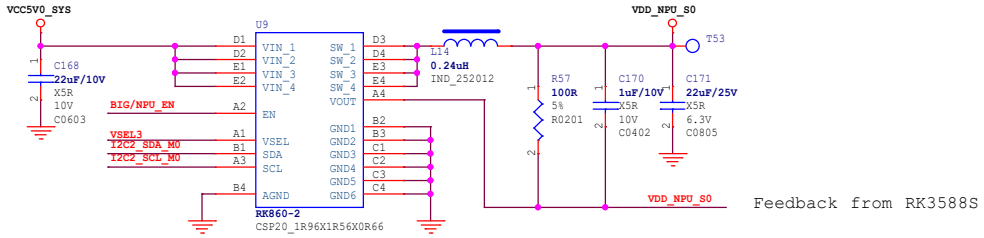
VDD_CPU_BIG0

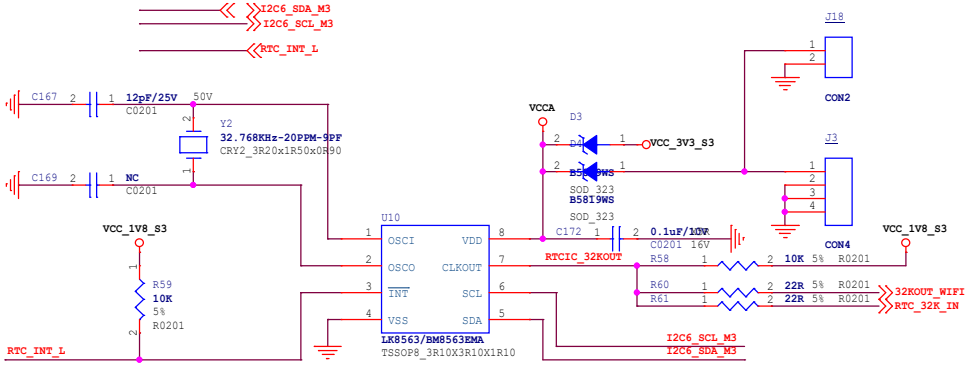


VDD_CPU_BIG1



VDD_NPU



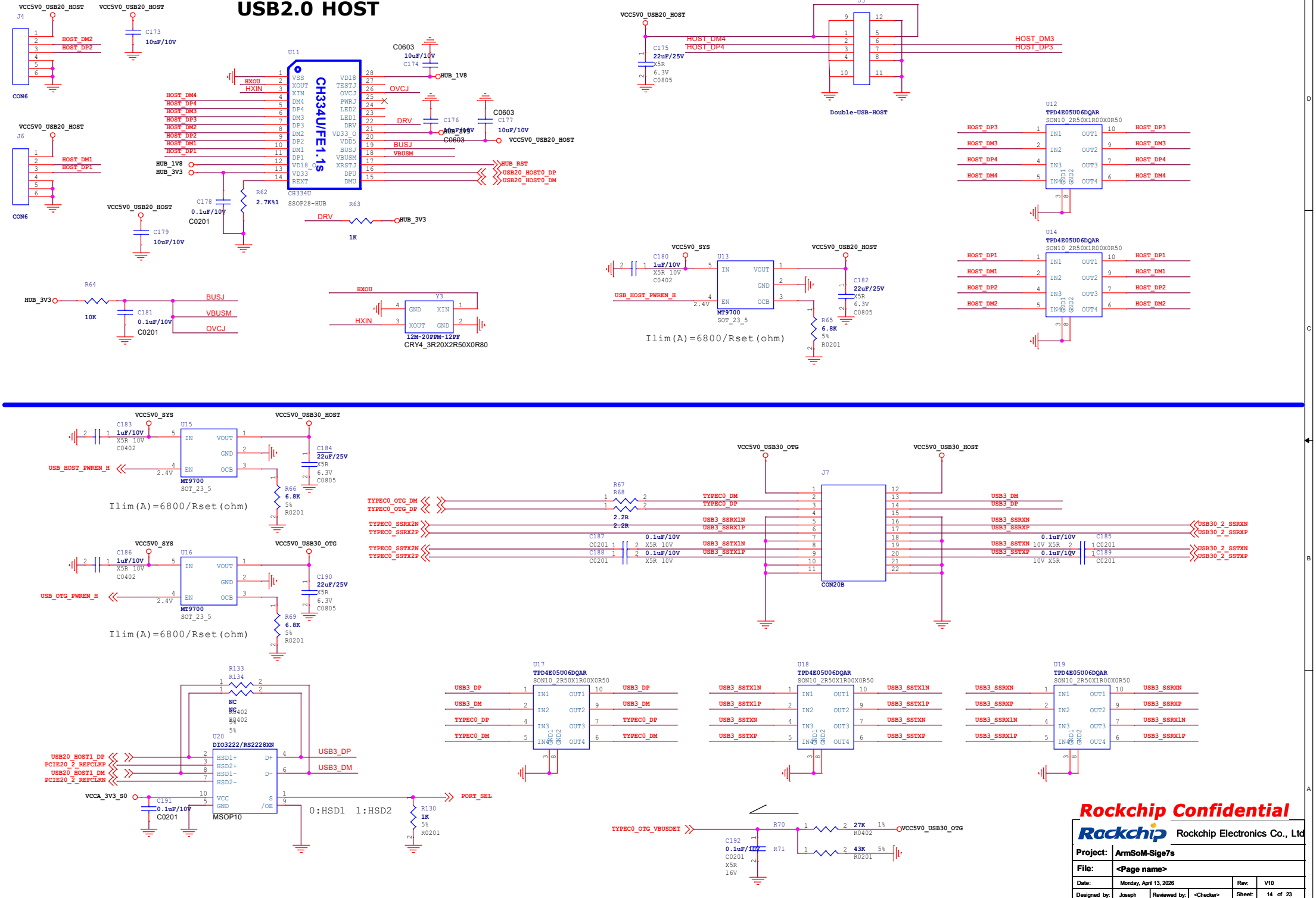




Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	13 of 23

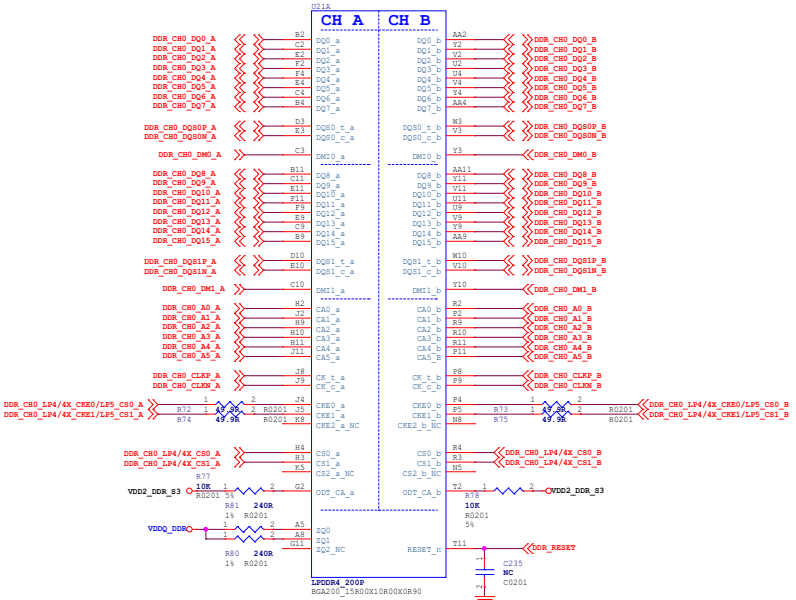
USB2.0 HOST

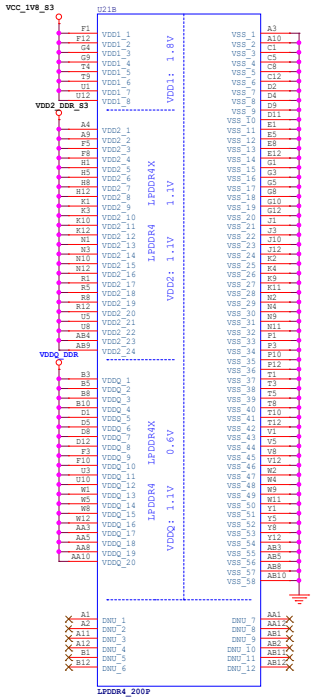


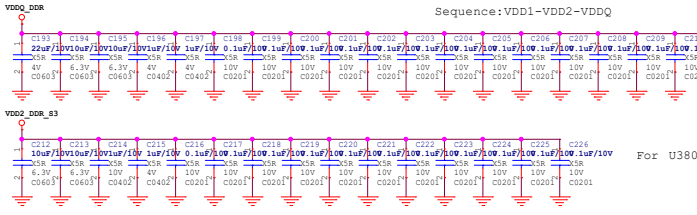
Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	14 of 23

DRAM-LPDDR4/4x_2X32bit

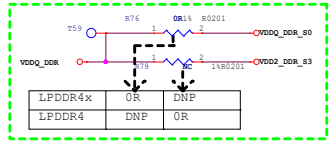




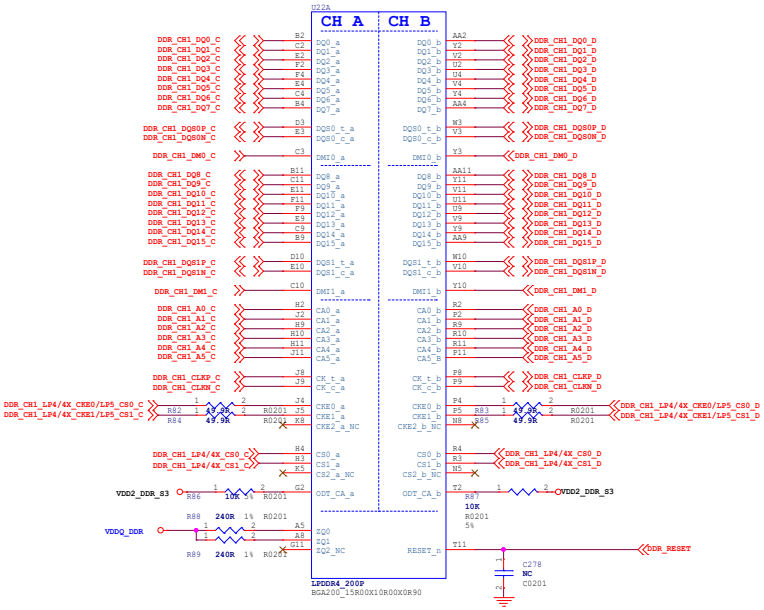


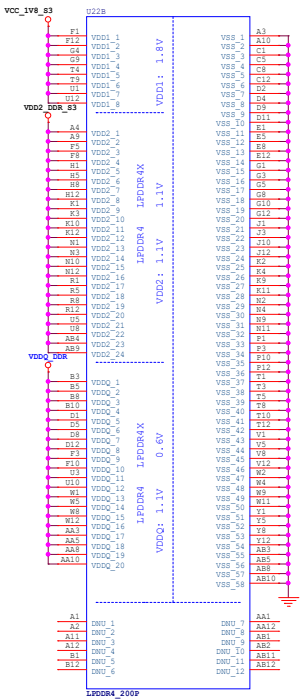
Sequence:VDD1-VDD2-VDDQ

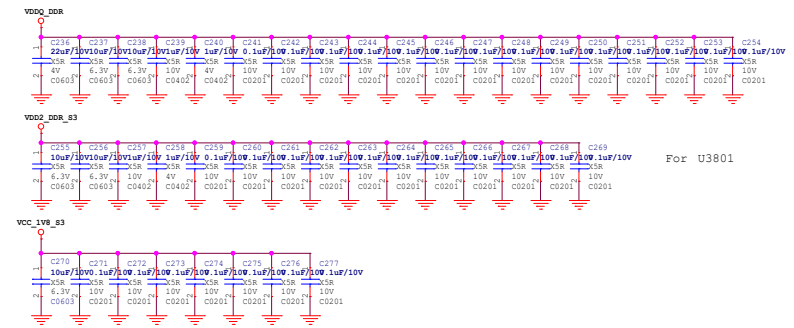
	LPDDR4	LPDDR4X
VDD1:	1.70-1.95	1.70-1.95
VDD2:	1.06-1.17	1.06-1.17
VDDQ:	1.06-1.17	0.57-0.65



LPDDR4x	0R	DNP
LPDDR4	DNP	0R



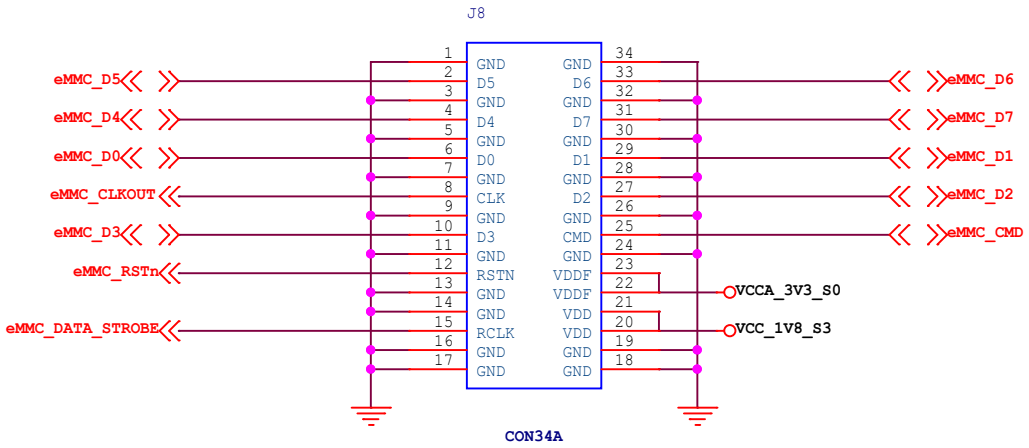


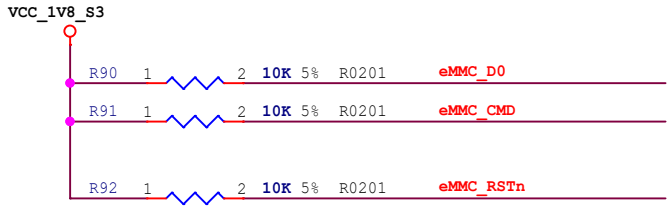


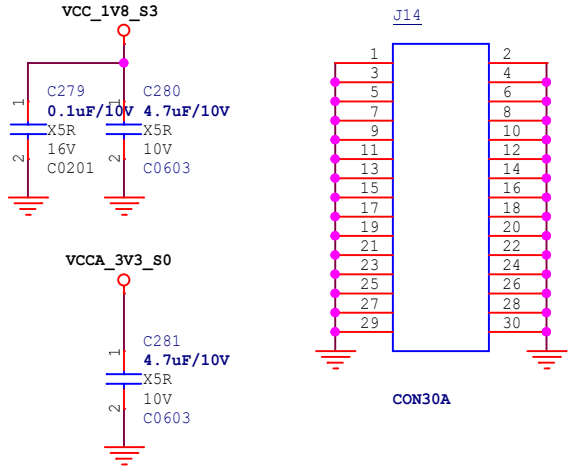
Rockchip Confidential

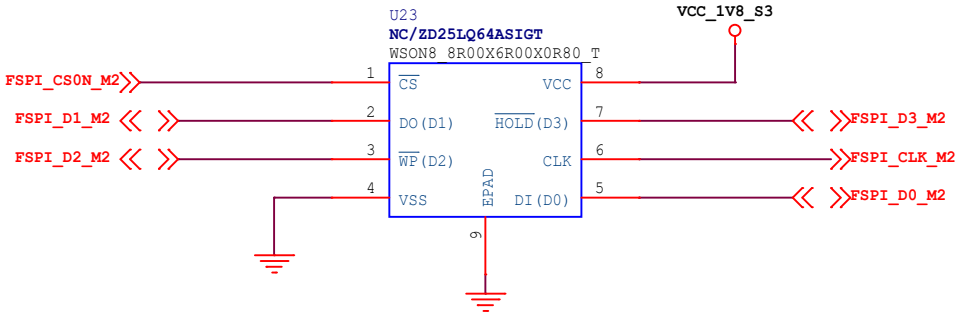
Rockchip Electronics Co., Ltd			
Project:	ArmSoM-Sige7s		
File:	<Page name>		
Date:	Monday, April 13, 2026	Rev:	V10
Designed by:	Joseph	Reviewed by: <Checker>	Sheet: 15 of 23

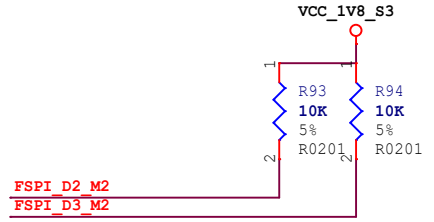
eMMC Flash

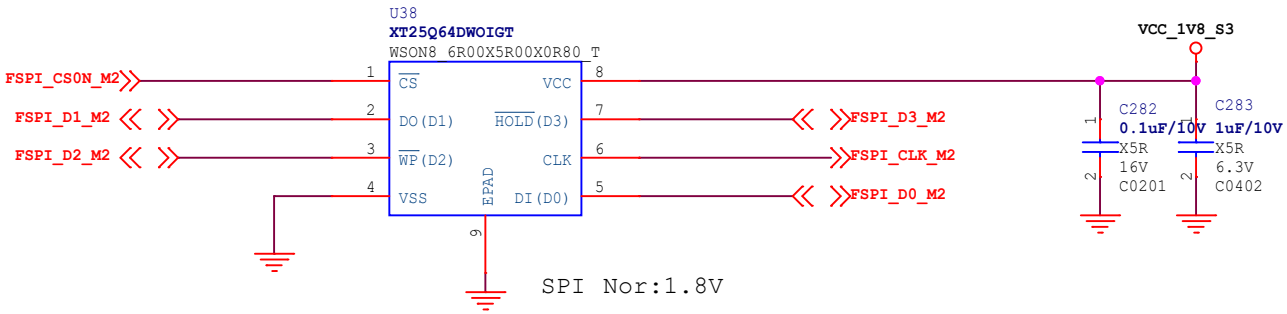








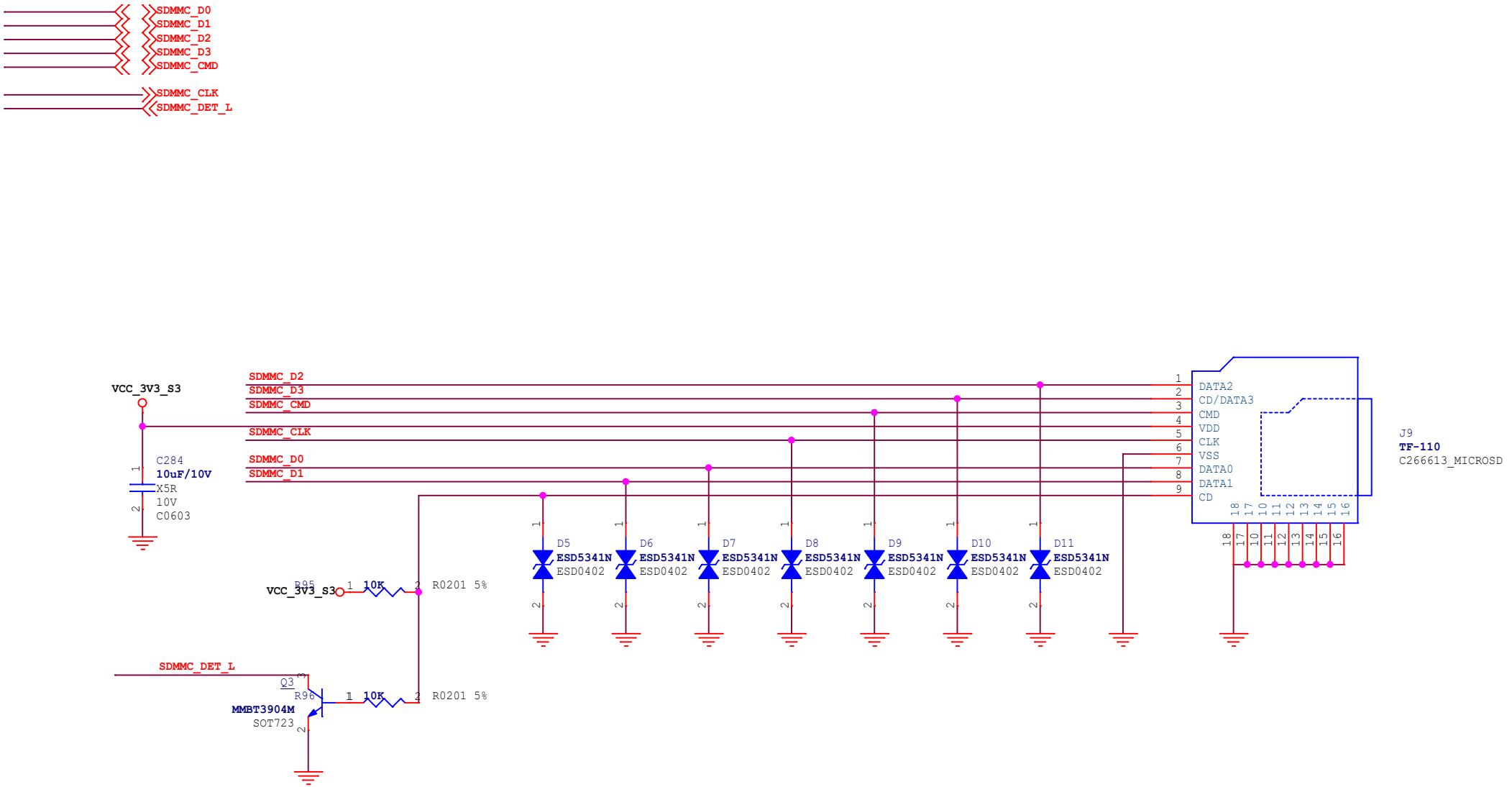




Rockchip Confidential

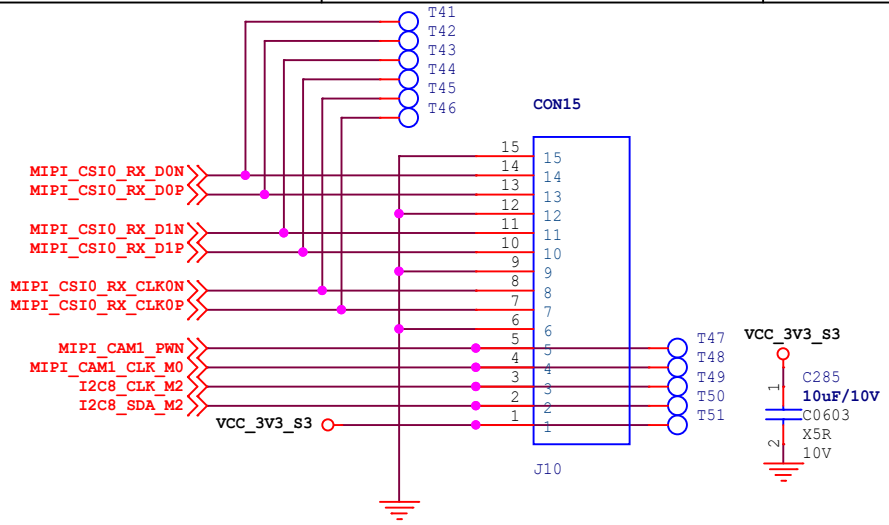
Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	16 of 23

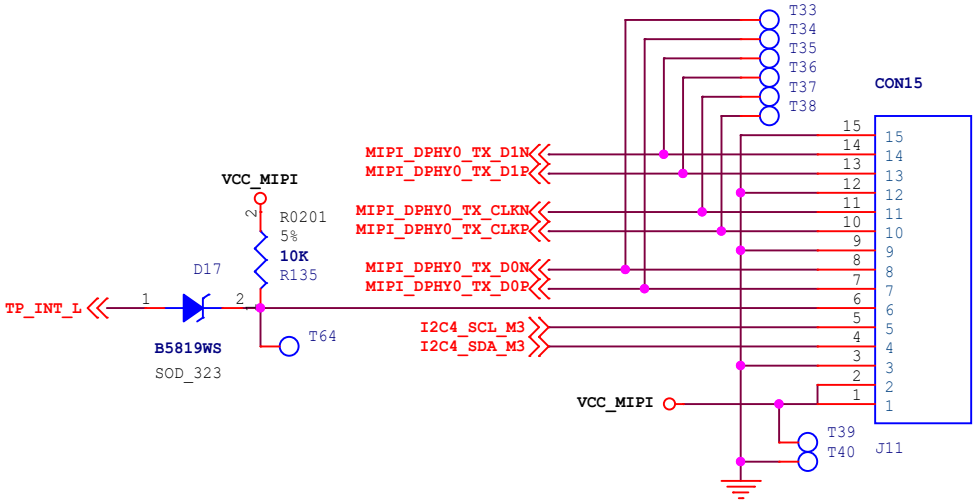
MicroSD Card

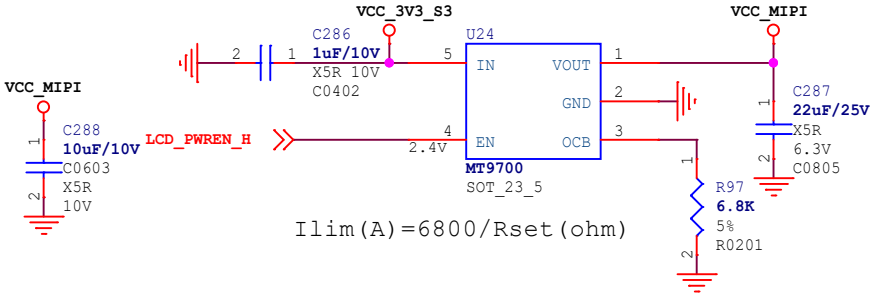


Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	17 of 23



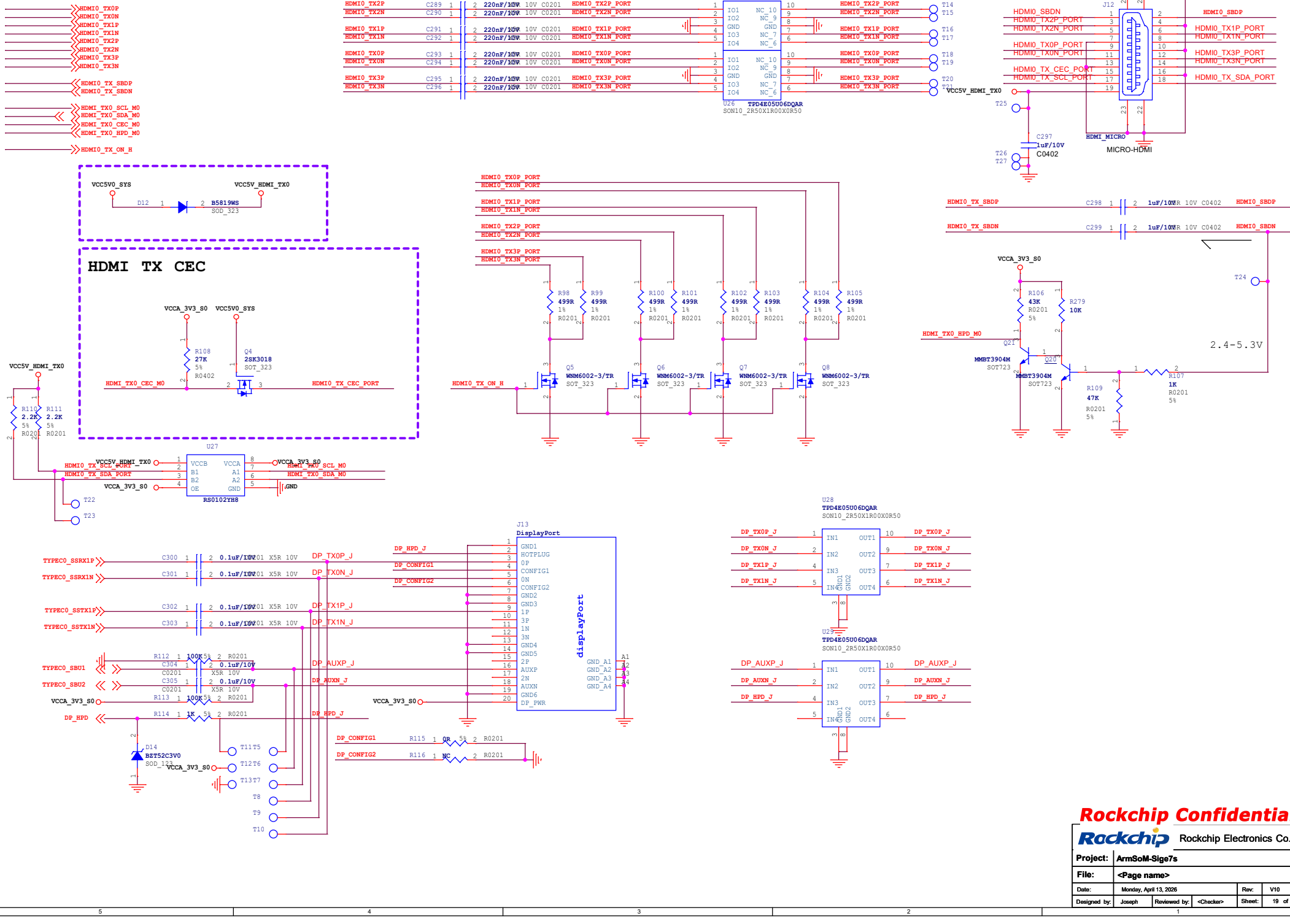




Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	18 of 23

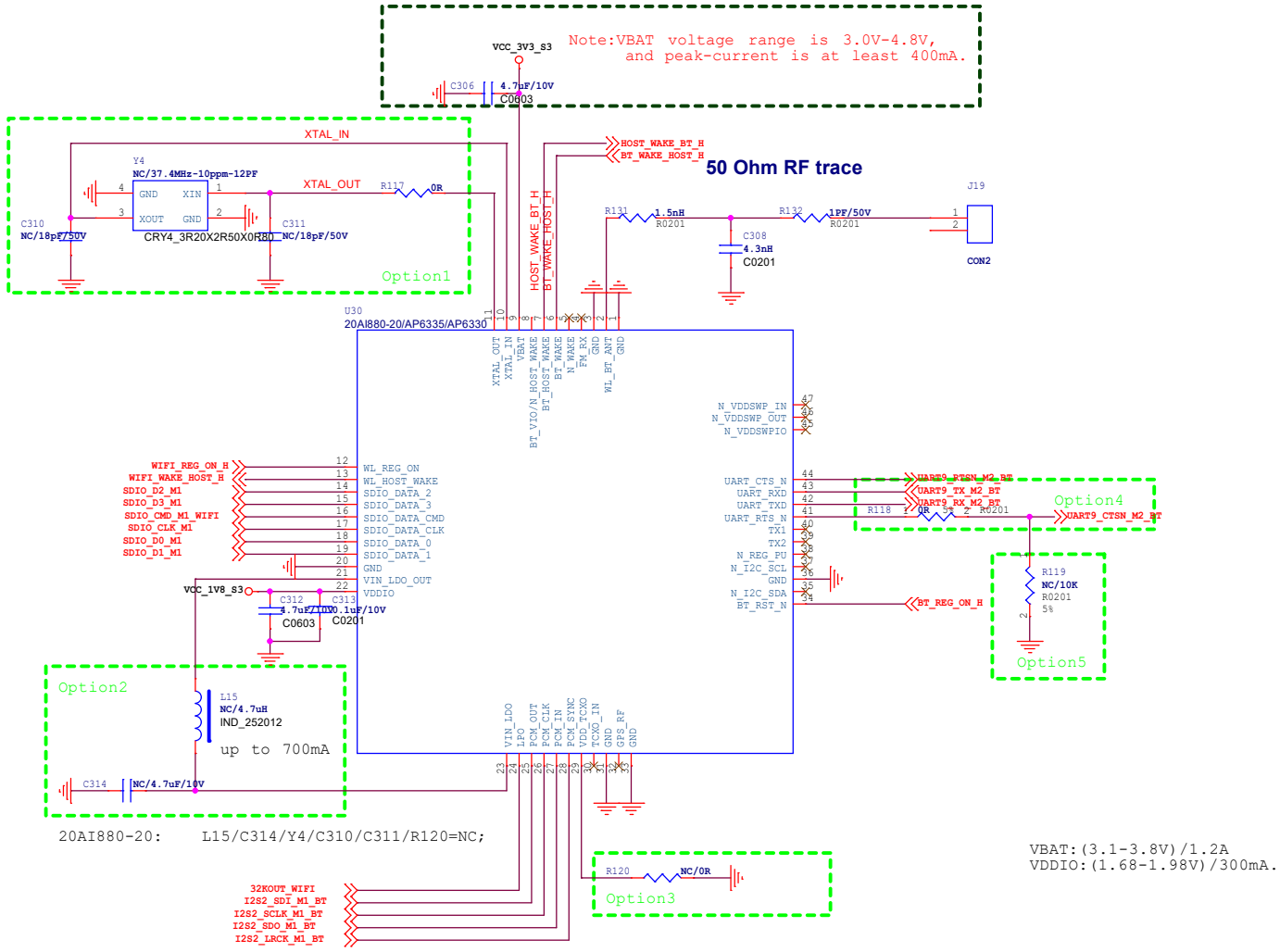
HDMI2.1 TX0



Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	19 of 23

PCIe WIFI6/BT Module-2T2R



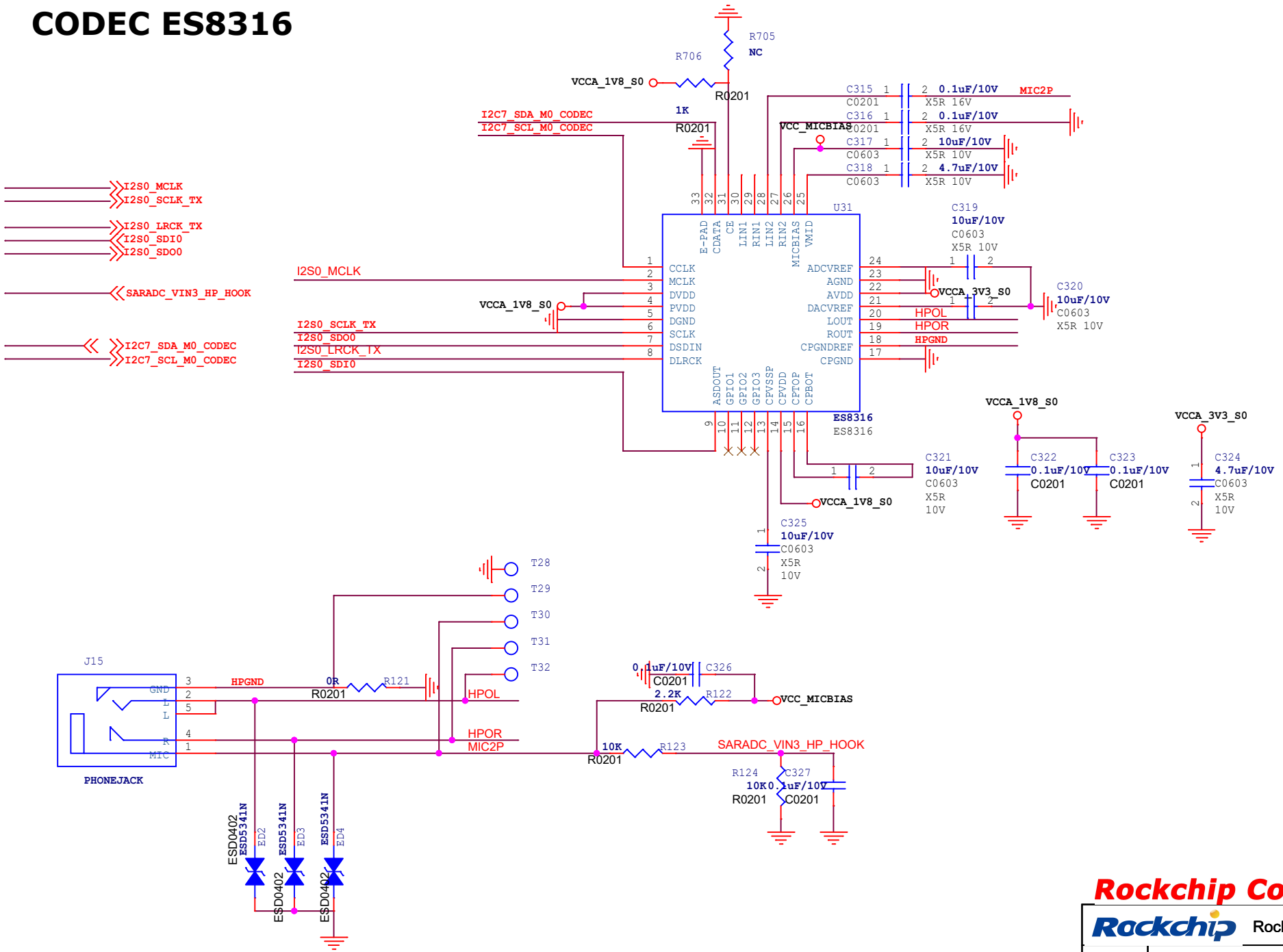
20AI880-20: L15/C314/Y4/C310/C311/R120=NC;

VBAT:(3.1-3.8V)/1.2A
VDDIO:(1.68-1.98V)/300mA.

Rockchip Confidential

Rockchip	Rockchip Electronics Co., Ltd				
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	20 of 23

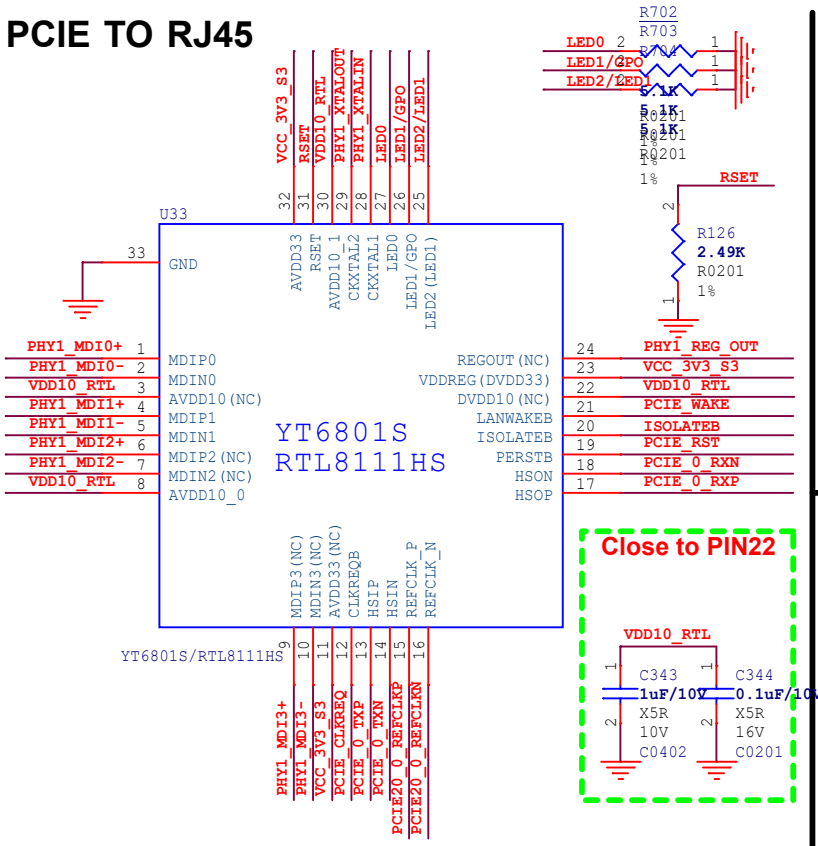
CODEC ES8316



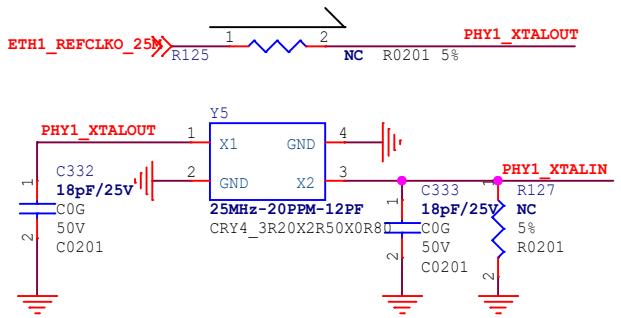
Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	Default	Sheet:	21 of 23

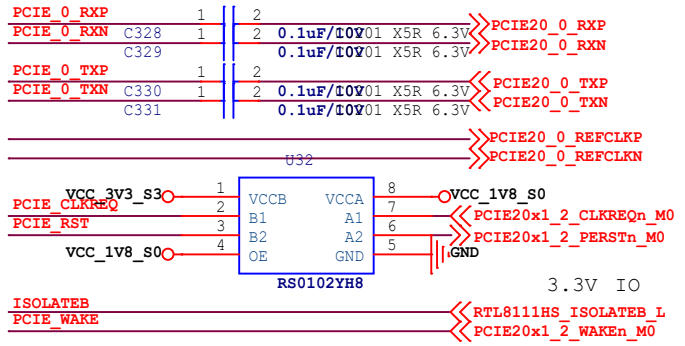
PCIE TO RJ45



Close to PIN22



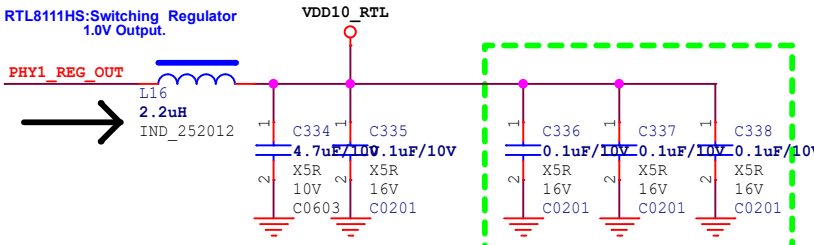
CKXTAL1(I): Input of 25Mhz Clock Reference.
CKXTAL2(IO): Input of External Clock Source
Output of 25Mhz Clock Reference.



LANWAKEB:Power Management Event (Open Drain;Active Low,1.8V/3.3V compatible input/output mode with a weak external pull resistor)

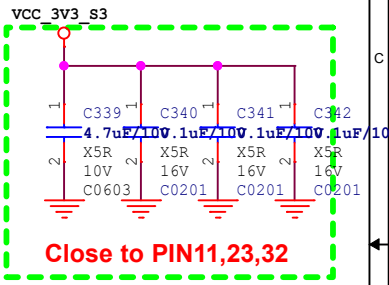
ISOLATEB :Isolate Pin(Active Low, 1.8V/3,3V compatible input)Used to isolate the RTL8111HS from the PCI Express bus,The RTL8111HS will not drive its PCI Express input as long as the Isolate pin is asserted.

RTL8111HS:Switching Regulator 1.0V Output.

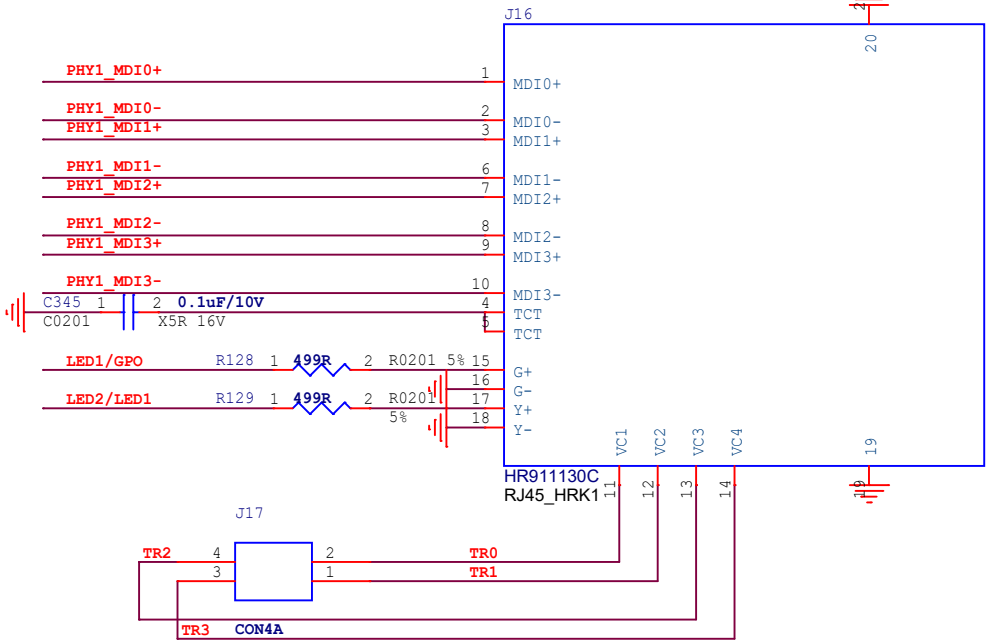


RTL8111HS:Switching Regulator 1.0V Output.
RTL8111H: LDO Regulator 1.0V Output.

Close to PIN3,8,30



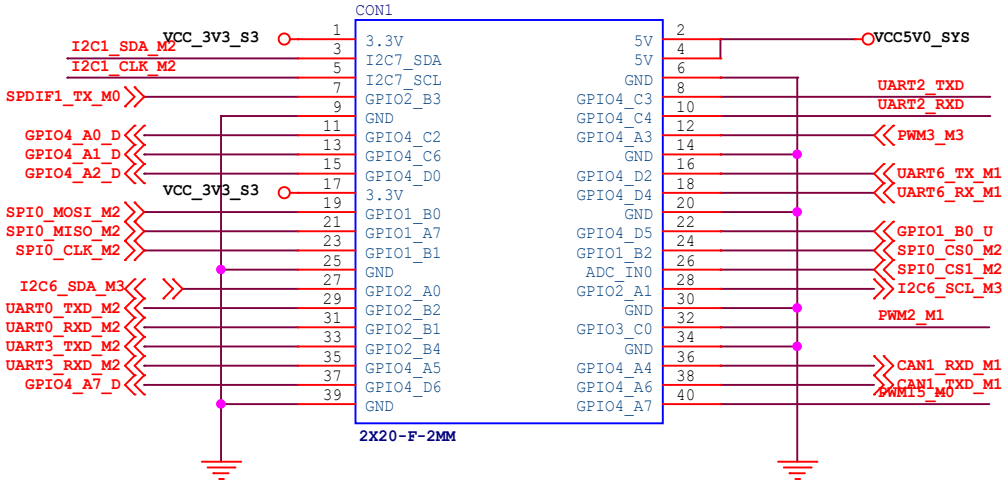
Close to PIN11,23,32

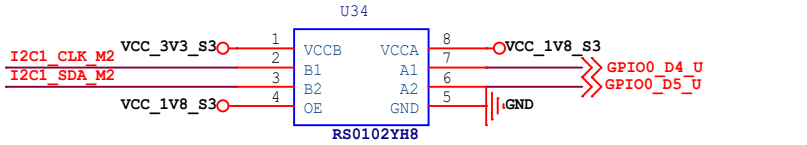


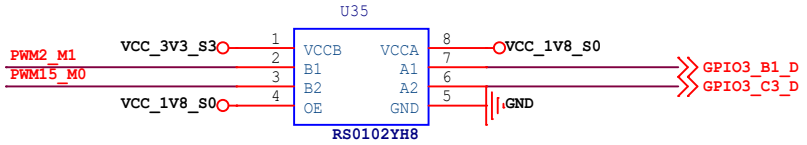
Rockchip Confidential

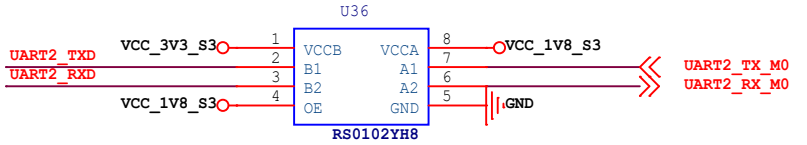
Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V1.1
Designed by:	Zhangdz	Reviewed by:	Default	Sheet:	22 of 23

UART Debug









Rockchip Confidential

Rockchip Electronics Co., Ltd					
Project:	ArmSoM-Sige7s				
File:	<Page name>				
Date:	Monday, April 13, 2026			Rev:	V10
Designed by:	Joseph	Reviewed by:	<Checker>	Sheet:	23 of 23